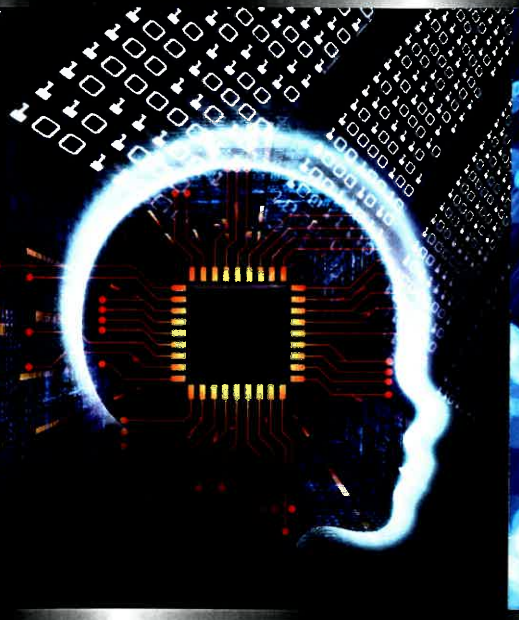
Module 05

FOR B2 CERTIFICATION

DIGITAL TECHNIQUES ELECTRONIC INSTRUMENT SYSTEMS

Avionics Maintenance Technician Certification Series



- Electronic Instrument Systems
- Numbering Systems
- Data Conversion
- Data Buses
- Logic Circuits
- Basic Computer Structure
- Microprocessors
- Integrated Circuits
- Multiplexing
- Fiber Optics
- Electronic Displays
- Electrostatic Sensitive Devices
- Software Management Control
- Electromagnetic Environment
- Typical Electronic/Digital Aircraft Systems

COMPLIANT WITH EASA

European Aviation Safety Agency

EASA PART 66/147

Version 002.2

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AVIONICS MAINTENANCE TECHNICIAN CERTIFICATION SERIES

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We wish you good luck and success in your studies and in your aviation career!

REVISION LOG

VERSION	EFFECTIVE DATE	DESCRIPTION OF CHANGE
001	2015 01	Module Creation and Release
002	2017 02	Format Update
002.1	2019 11	Corrections to Figures: 3-5, 5-14, 8-4, 9-4
002.2	2022 06	Addition of Measurement Standards and minor formatting updates.

MODULE EDITIONS AND UPDATES

ATB EASA Modules are in a constant state of review for quality, regulatory updates, and new technologies. This book's edition is given in the revision log above. Update notices will be available Online at www.actechbooks.com/revisions.html
If you would like to be notified when changes occur, please join our mailing list at www.actechbooks.com

MEASUREMENT STANDARDS

SI Units

Measurements in this book are presented with International System of Units (SI) standards in all cases except when otherwise specified by ICAO (for example, altitude expressed in feet or performance numbers as specified by a manufacturer). The chart below can be used should your studies call for conversions into imperial numbers.

Number Groups

This book uses the International Civil Aviation Organization (ICAO) standard of writing numbers. This method separates groups of 3 digits with a space, versus the European method by periods and the American method by commas. For example, the number one million is expressed as:

ICAO Standard	1 000 000
European Standard	1.000.000
American Standard	1,000,000

Prefixes

The prefixes in the table below form names of the decimal equivalents in SI units.

MULTIPLICATION FACTOR	PREFIX	SYMBOL
1 000 000 000 000 000 000 = 10^{18}	exa	E
1 000 000 000 000 000 = 10^{15}	peta	P
1 000 000 000 000 = 10^{12}	tera	T
1 000 000 000 = 10^{9}	giga	G
1 000 000 = 10^{6}	mega	M
1 000 = 10^{3}	kilo	k
100 = 10^{2}	hecto	h
10 = 10^{1}	deca	da
0.1 = 10^{-1}	deci	d
0.0 1 = 10^{-2}	centi	c
0.001 = 10^{-3}	milli	m
0.000 001 = 10^{-6}	micro	μ
0.000 000 001 = 10^{-9}	nano	n
0.000 000 000 001 = 10^{-12}	pico	p
0.000 000 000 000 001 = 10^{-15}	femto	f
0.000 000 000 000 000 001 = 10^{-18}	atto	a

COMMON CONVERSIONS

IMPERIAL SYSTEM	TO	SI (METRIC)
Distance		
1 Inch	is equal to	2.54 Centimeters
1 Foot	is equal to	0.304 Meters
1 (Statute) Mile	is equal to	1.609 Kilometers
Weight		
1 Pound	is equal to	0.454 Kilograms
Volume		
1 Quart	is equal to	0.946 Liters
1 Gallon	is equal to	3.785 Liters
Temperature		
°0 Fahrenheit	is equal to	(-)17.778 Celsius (°C)
°0 Fahrenheit	is equal to	255.37 Kelvin (K)
Area		
1 Square Inch	is equal to	6.451 Square Centimeters
1 Square Foot	is equal to	0.093 Square Meters
1 Square Mile	is equal to	2.59 Square Kilometers
Velocity		
1 Foot Per Second	is equal to	0.304 Meters Per Second
1 Square Inch	is equal to	1.609 Kilometers Per Hour
1 Square Inch	is equal to	1.852 Kilometers Per Hour

SI (METRIC)	TO	IMPERIAL SYSTEM
Distance		
1 Centimeter	is equal to	0.394 Inches
1 Meter	is equal to	3.28 Feet
1 Kilometer	is equal to	0.621 Miles
Weight		
1 Kilogram	is equal to	2.204 Pounds
Volume		
1 Liter	is equal to	1.057 Quarts
1 Liter	is equal to	0.264 Gallons
Temperature		
°0 Celsius (°C)	is equal to	33.8° Fahrenheit
°0 Kelvin (K)	is equal to	(-)437.87 Fahrenheit
Area		
1 Square Centimeter	is equal to	0.155 Square Inches
1 Square Meter	is equal to	10.764 Square Feet
1 Square Kilometer	is equal to	0.386 Square Miles
Velocity		
1 Meter Per Second	is equal to	3.281 Feet Per Second
1 Kilometer Per Hour	is equal to	0.621 Miles Per Hour
1 Kilometer Per Hour	is equal to	0.540 Knots

Pressure		
pounds per square inch (psi)	kiloPascals (kPa)	6.988
pounds per square inch (psi)	Pascals (Pa)	6.895

EASA LICENSE CATEGORY CHART

Module Number and Title		A1 Airplane Turbine	B1.1 Airplane Turbine	B1.2 Airplane Piston	B1.3 Helicopter Turbine	B1.4 Helicopter Piston	B2 Avionics
1	Mathematics	X	X	X	X	X	X
2	Physics	X	X	X	X	X	X
3	Electrical Fundamentals	X	X	X	X	X	X
4	Electronic Fundamentals		X	X	X	X	X
5	Digital Techniques / Electronic Instrument Systems	X	X	X	X	X	X
6	Materials and Hardware	X	X	X	X	X	X
7A	Maintenance Practices	X	X	X	X	X	X
8	Basic Aerodynamics	X	X	X	X	X	X
9A	Human Factors	X	X	X	X	X	X
10	Aviation Legislation	X	X	X	X	X	X
11A	Turbine Aeroplane Aerodynamics, Structures and Systems	X	X				
11B	Piston Aeroplane Aerodynamics, Structures and Systems			X			
12	Helicopter Aerodynamics, Structures and Systems				X	X	
13	Aircraft Aerodynamics, Structures and Systems						X
14	Propulsion						X
15	Gas Turbine Engine	X	X		X		
16	Piston Engine			X		X	
17A	Propeller	X	X	X			

GENERAL KNOWLEDGE REQUIREMENTS

MODULE 05 SYLLABUS AS OUTLINED IN PART-66, APPENDIX 1

Level 1
A familiarization with the principal elements of the subject.
Objectives:
a. The applicant should be familiar with the basic elements of the subject.
b. The applicant should be able to give a simple description of the whole subject, using common words and examples.
c. The applicant should be able to use typical terms.

Level 2
A general knowledge of the theoretical and practical aspects of the subject and an ability to apply that knowledge.
Objectives:
a. The applicant should be able to understand the theoretical fundamentals of the subject.
b. The applicant should be able to give a general description of the subject using, as appropriate, typical examples.
c. The applicant should be able to use mathematical formula in conjunction with physical laws describing the subject.
d. The applicant should be able to read and understand sketches, drawings and schematics describing the subject.
e. The applicant should be able to apply his knowledge in a practical manner using detailed procedures.

Level 3
A detailed knowledge of the theoretical and practical aspects of the subject and a capacity to combine and apply the separate elements of knowledge in a logical and comprehensive manner.
Objectives:
a. The applicant should know the theory of the subject and interrelationships with other subjects.
b. The applicant should be able to give a detailed description of the subject using theoretical fundamentals and specific examples.
c. The applicant should understand and be able to use mathematical formula related to the subject.
d. The applicant should be able to read, understand and prepare sketches, simple drawings and schematics describing the subject.
e. The applicant should be able to apply his knowledge in a practical manner using manufacturer's instructions.
f. The applicant should be able to interpret results from various sources and measurements and apply corrective action where appropriate.

PART-66 - APPENDIX I
BASIC KNOWLEDGE REQUIREMENTS

	LEVELS B2
Sub-Module 01 - Electronic Instrument Systems	
Typical systems arrangements and cockpit layout of electronic instrument systems.	3
Sub-Module 02 - Numbering Systems	
Numbering systems: binary, octal and hexadecimal; Demonstration of conversions between the decimal and binary, octal and hexadecimal systems and vice versa.	2
Sub-Module 03 - Data Conversion	
Analog Data, Digital Data; Operation and application of analog to digital, and digital to analogue converters, inputs and outputs, limitations of various types.	2
Sub-Module 04 - Data Buses	
Operation of data buses in aircraft systems, including knowledge of ARINC and other specifications. Aircraft Network/Ethernet.	2
Sub-Module 05 - Logic Circuits	
(a) Identification of common logic gate symbols, tables and equivalent circuits; Applications used for aircraft systems, schematic diagrams.	2
(b) Interpretation of logic diagrams.	2
Sub-Module 06 - Basic Computer Structure	
(a) Computer terminology (including bit, byte, software, hardware, CPU, IC, and various memory devices such as RAM, ROM, PROM); Computer technology (as applied in aircraft systems).	-
(b) Computer related terminology; Operation, layout and interface of the major components in a micro computer including their associated bus systems; Information contained in single and multiaddress instruction words; Memory associated terms; Operation of typical memory devices; Operation, advantages and disadvantages of the various data storage systems.	2
Sub-Module 07 - Microprocessors	
Functions performed and overall operation of a microprocessor; Basic operation of each of the following microprocessor elements: control and processing unit, clock, register, arithmetic logic unit.	2
Sub-Module 08 - Integrated Circuits	
Operation and use of encoders and decoders; Function of encoder types; Uses of medium, large and very large scale integration.	2

Sub-Module 09 - Multiplexing

Operation, application and identification in logic diagram of multiplexers and demultiplexers. 2

Sub-Module 10 - Fiber Optics

Advantages and disadvantages of fiber optic data transmission over electrical wire propagation; 2
Fiber optic data bus;
Fiber optic related terms;
Terminations;
Couplers, control terminals, remote terminals;
Application of fiber optics in aircraft systems.

Sub-Module 11 - Electronic Displays

Principles of operation of common types of displays used in modern aircraft, including Cathode Ray Tubes, Light Emitting Diodes and Liquid Crystal Display. 2

Sub-Module 12 - Electrostatic Sensitive Devices

Special handling of components sensitive to electrostatic discharges; 2
Awareness of risks and possible damage, component and personnel anti-static protection devices.

Sub-Module 13 - Software Management Control

Awareness of restrictions, airworthiness requirements and possible catastrophic effects of unapproved changes to software programs. 2

Sub-Module 14 - Electromagnetic Environment

Influence of the following phenomena on maintenance practices for electronic system: 2
-EMC-Electromagnetic Compatibility
-EMI-Electromagnetic Interference
-HIRF-High Intensity Radiated Field
-Lightning/lightning protection

Sub-Module 15 - Typical Electronic/Digital Aircraft Systems

General arrangement of typical electronic/digital aircraft systems and associated BITE (Built In Test Equipment) such as: 2
For B1 and B2 only:
ACARS-Aircraft Communication and Addressing and Reporting System, EICAS-Engine Indication and Crew Alerting System, FBW-Fly by Wire, FMS-Flight Management System, IRS-Inertial Reference System,

For B1, B2 and B3:
ECAM-Electronic Centralised Aircraft Monitoring, EFIS-Electronic Flight Instrument System, GPS-Global Positioning System, TCAS-Traffic Alert Collision Avoidance System, Integrated Modular Avionics, Cabin Systems, Information Systems.

DIGITAL TECHNIQUES ELECTRONIC INSTRUMENT SYSTEMS

SUB-MODULE 01
ELECTRONIC INSTRUMENT SYSTEMS

SUB-MODULE 02
NUMBERING SYSTEMS

SUB-MODULE 03
DATA CONVERSION

SUB-MODULE 04
DATA BUSES

SUB-MODULE 05
LOGIC CIRCUITS

SUB-MODULE 06
BASIC COMPUTER STRUCTURE

CONTENTS

SUB-MODULE 13
SOFTWARE MANAGEMENT CONTROL

SUB-MODULE 14
ELECTROMAGNETIC ENVIRONMENT

SUB-MODULE 15
TYPICAL ELECTRONIC/DIGITAL AIRCRAFT SYSTEMS

PART-66 SYLLABUS LEVELS

CERTIFICATION CATEGORY → B2

Sub-Module 01

ELECTRONIC INSTRUMENT SYSTEMS

Knowledge Requirements

5.1 - Electronic Instrument Systems

Typical systems arrangements and cockpit layout of electronic instrument systems.	3

5.1 - ELECTRONIC INSTRUMENT SYSTEMS

Instruments that aid the pilot in controlling the altitude, attitude, airspeed and heading of the aircraft are known as flight instruments. Since the early days of flight there have been four basic flight instruments that have formed the well-known "T" arrangement located in the center of the instrument panel, as shown in ***Figure 1-1.*** These four basic instruments are 1) the airspeed indicator, located on the top left, that measures the aircraft's speed in nautical miles per hour; 2) the attitude indicator, located on top center, that shows the aircraft's attitude relative to the earth's horizon; 3) the altimeter, on the top right, that displays the barometric altitude as measured in feet; and 4) the gyro-slaved heading indicator, in the bottom center, which shows which direction the aircraft is flying.

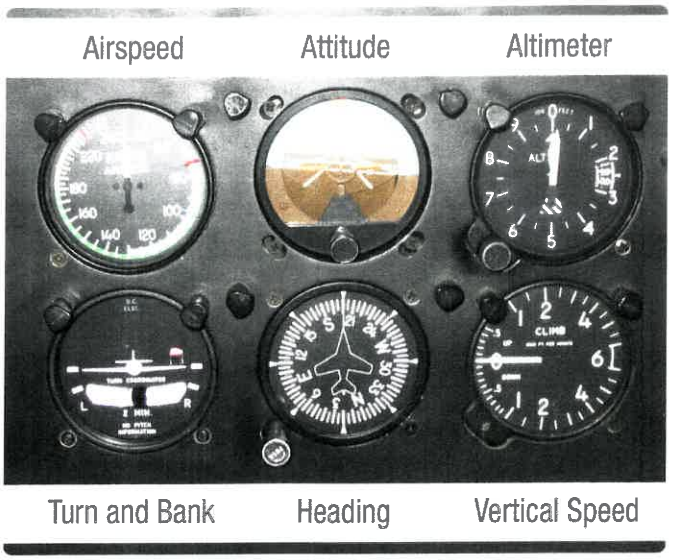


Figure 1-1. Basic analog cockpit flight instruments.

These four basic flight instruments are typically augmented with a turn-and-bank indicator that displays the rate of turn in the roll axis and amount of bank in the yaw axis, and a vertical speed indicator that displays the rate of ascent or descent in feet per minute. Assuming that the aircraft has radio navigation aids, it will also come equipped with a Radio Magnetic Indicator (RMI) coupled to an Automatic Direction Finder (ADF), and a Course Deviation Indicator (CDI) driven by VHF Omnidirectional Range (VOR) and Instrument Landing System (ILS) receivers. The ILS receiver drives the glideslope needle to set the glide path on an instrument approach and localizer needle provides lateral guidance to the center of the runway. A VHF Marker Beacon may be used in conjunction with the ILS to indicate position along the approach to the runway.

ANALOG INSTRUMENTS

These early flight instruments were analog meaning that they contained either mechanical or electro-mechanical rotating mechanisms to drive the pointer dials on the instruments. For example, an analog airspeed indicator receives air pressure from the pitot tube, which expands a bellows that turns the dial on the indicator. With a digital system, the pitot air pressure enters an air data computer that converts the analog information into a digital data stream. Digital data is then sent to the airspeed indicator via an aircraft data bus where the data is converted back into analog signals to drive a pointer dial and/or is displayed digitally in numbers.

DIGITAL INSTRUMENTS

With the advent of digital electronics in the early 1970's, Electronic Instrument Systems, also known as "glass cockpits", evolved that were more much more reliable than mechanical or electro-mechanical analog instruments, and had the advantage of combining several flight and navigation functions into one display to provide the crew with greater situational awareness.

The first commercial transport aircraft to employ an Electronic Instrument System (EIS) was the McDonnell Douglas MD-80 in 1979. The EIS on the MD-80 used Cathode Ray Tube (CRT) technology. However, during the next 10 years, Liquid Crystal Display (LCD) technology matured thereby replacing CRTs. Flat-panel LCDs are lighter than CRT displays, require less volume, and consume less electrical power, thereby generating less cockpit heat. Glass cockpit configurations vary widely between aircraft models from a single flight and navigation display in a small private aircraft to five or more LCD displays in a commercial transport aircraft. (***Figure 1-2***)

ELECTRONIC DISPLAYS

The early EIS displays mimicked the analog display formats for ease in pilot training as the crew transitioned from older analog displays to digital displays that were driven by aircraft data computers, known as display processors or symbol generators.

Figure 1-2. Airbus A380 EIS with 8 large LCD displays.

Figure 1-3. Equivalent Electromechanical Flight and Navigation Instruments on the left.

Figure 1-3 depicts an early model Boeing 737 instrument panel with an analog Attitude Direction Indicator (ADI) and analog Horizontal Situation Display (HSI) in the left picture, and a later model B737 instrument panel with electronic ADI (EADI) and electronic HSI (EHSI) displays shown in the right picture.

The ADI or EADI is an artificial horizon with lateral bars superimposed to display computer-generated pitch, roll and bank steering commands from the Flight Director computer. The HSI or EHSI is similar to a heading indicator, except that it combines navigation commands from the VHF Omni-Range (VOR) or Global Positioning System (GPS) receivers which are used for en-route guidance, or from the Instrument Landing System (ILS), which is used for terminal guidance. Besides heading, the HSI/EHSI also provides actual track, desired track, track angle error, drift angle, cross-track deviation, and distance to destination information from the Distance Measuring Equipment (DME) or Inertial Navigation System (INS). (***Figure 1-4***)

The pilot and the co-pilot not only have independent EADI and EHSI displays, but they also have independent Display Processor Units, also known as Symbol Generators, to drive their displays (***Figure 1-5***). Display formats are produced by the Symbol Generators that receive inputs from the crew and various on-board systems. The Flight Director Systems, Navigation Systems, Air Data Systems, and Weather Radar provide inputs to the Symbol Generators, along with commands from the each crewmember's display control panel. The Symbol Generators produce the graphics for the EADI, EHSI, and an optional Multi-Function Display (MFD) that is mounted in the center instrument panel. The MFD, which is physically identical to the EADI and EHSI, is typically used to display weather radar information; however, it can also be used to display either flight information or navigational information in the event of an EADI or EHSI failure. The following section will discuss the Boeing 777 EIS, which is a more advanced example of the one just covered.

ELECTRONIC FLIGHT INSTRUMENT SYSTEM

The Boeing 777, which first entered service in 1995, has six 8' × 8" multi-color LCD displays as shown in ***Figure 1-6***. The B777 EIS consists of a dual-redundant Electronic Flight Instrument Systems (EFIS) and Engine Indication and Crew Alerting System (EICAS). On the left side of the instrument panel is the Captain's EFIS, consisting of a Primary Flight Display (PFD)

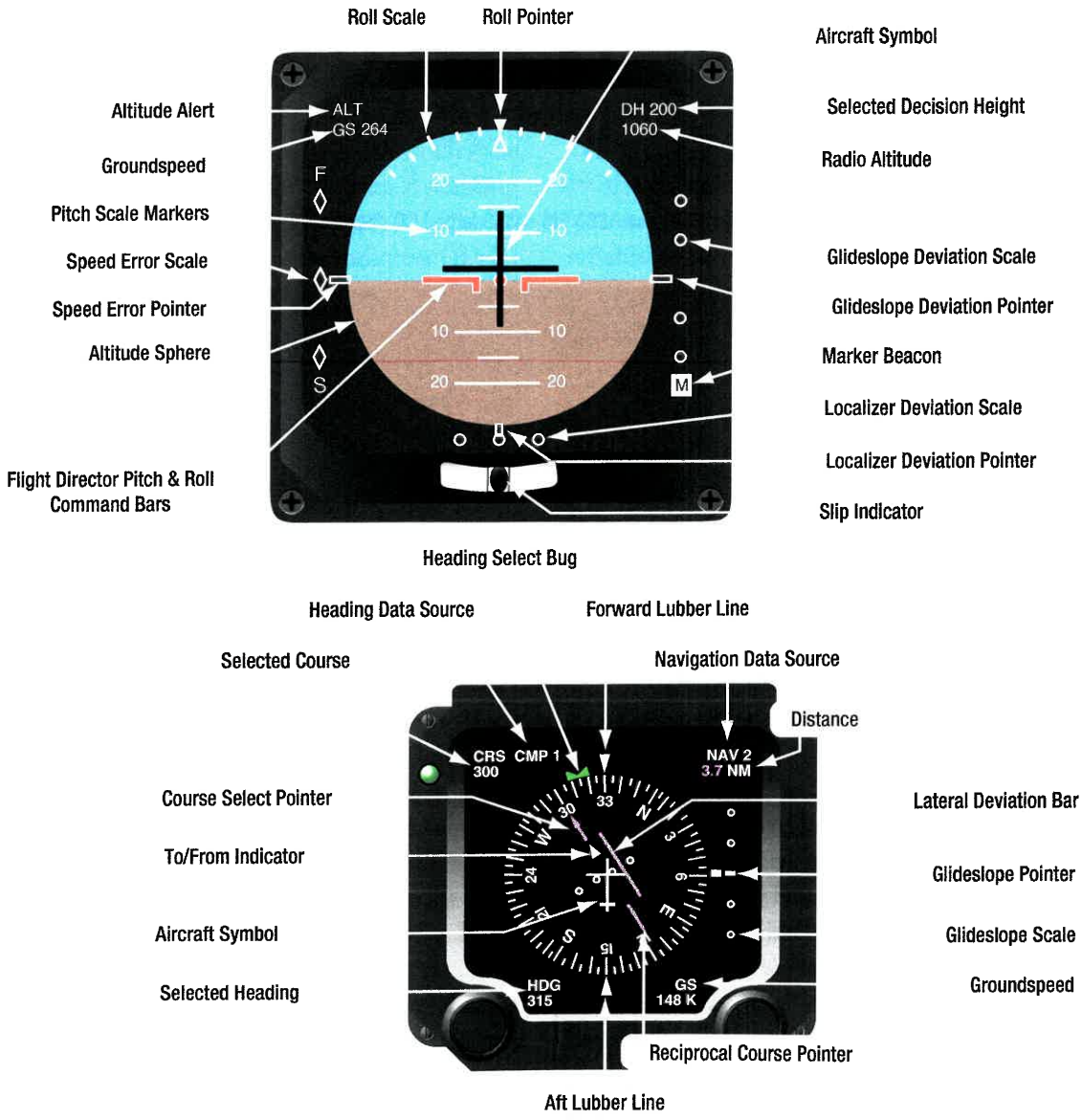


Figure 1-4. Typical EADI (top) and EHSI (bottom) Display Symbology.

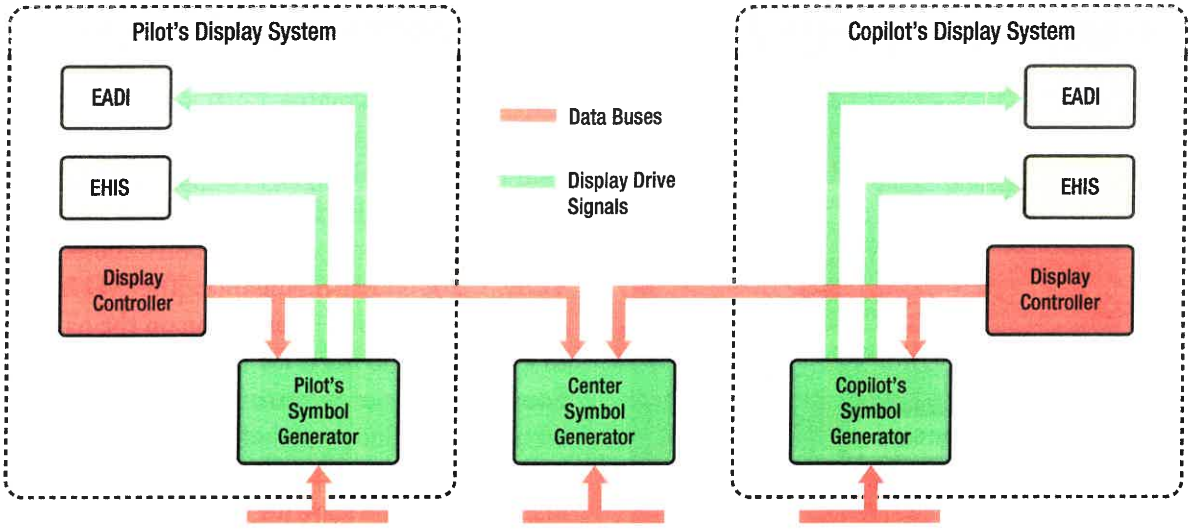


Figure 1-5. Electronic Displays are driven by Symbol Generators.

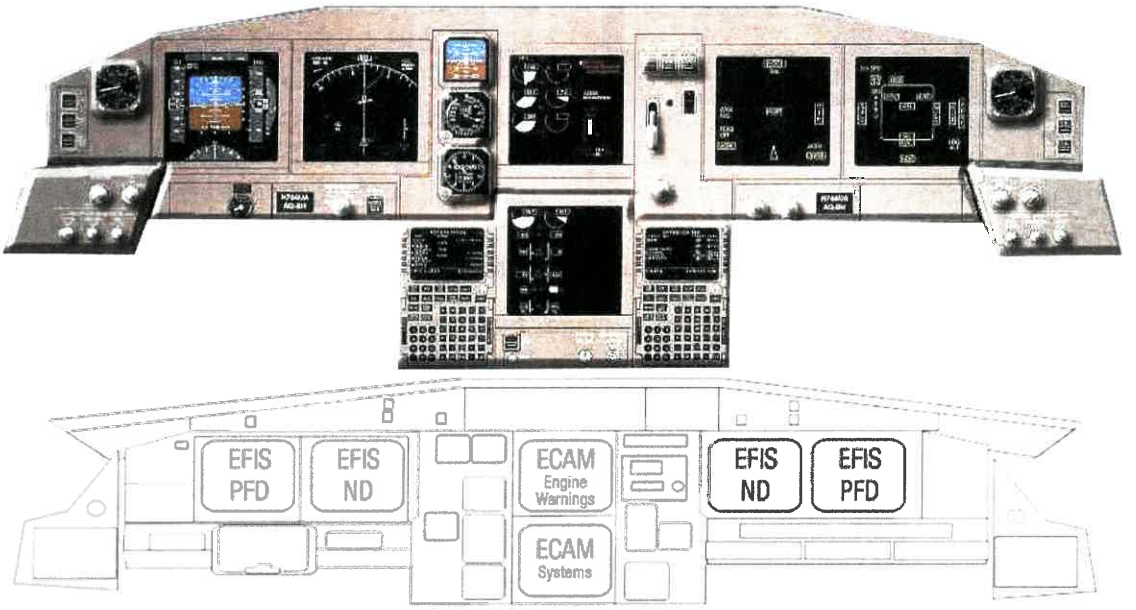


Figure 1-6. Boeing 777 Electronic Instrument System has 6 LCD Displays.

located outboard and a Navigation Display (ND) located inboard. The Co-Pilot's EFIS located on the right instrument panel has an identical PFD and ND, located outboard and inboard respectively. All the displays are interchangeable to reduce the number of required spares. The information shown on each display, whether for flight or navigation, is determined by what each crew member selects on their individual display control panels.

The PFD takes the place of the EADI and displays all the information critical to flight, including attitude, airspeed, barometric altitude, vertical speed, heading, flight modes, radio altitude, ILS data, and Traffic Alert and Collision Avoidance System (TCAS) resolution advisory. The PFDs are designed to increase the crew's situational awareness by integrating all of this information into a single composite display instead of the crew having to monitor several independent analog instruments. Also, the colors on the display change to alert the crew to potentially hazardous flight conditions, such as low airspeed, high rate of descent, etc.

Figure 1-7 is a typical Primary Flight Display format showing the artificial horizon in the center of the display, airspeed on the left side, altitude on the right side, heading on the bottom, and flight modes on the top of the display. Notice how the moving ladder format used for altitude and airspeed provide both absolute and

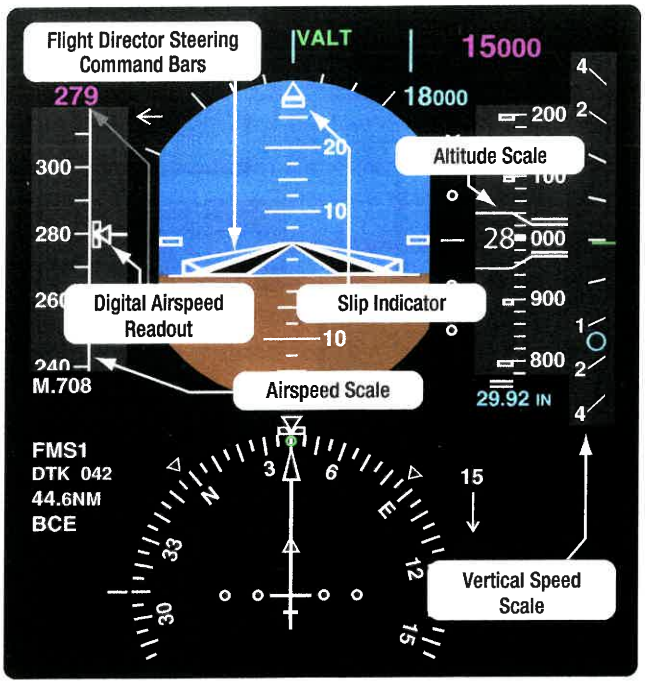


Figure 1-7. Primary flight display format.

relative information so the crew knows not only the exact numeric value, but also the rate that the altitude and airspeed is changing.

The Navigation Display, shown in ***Figure 1-8***, takes the place of the EHSI display to show the requisite information to navigate the aircraft, including heading, VOR, GPS, and ILS guidance. The ND has the ability to overlay additional information on the navigation page to eliminate the need for separate dedicated displays. Some examples of information that is typically overlaid on the ND include weather information from either the onboard weather radar (WXR) or ground based sensors, and digital maps showing pre-programmed routes and waypoints from the Flight Management System.

ENGINE INDICATION AND CREW ALERTING SYSTEM

The Boeing® Engine Indication and Crew Alerting System (EICAS), also called an Electronic Centralized Aircraft Monitor (ECAM) on Airbus aircraft, performs the monitoring of aircraft systems that was previously

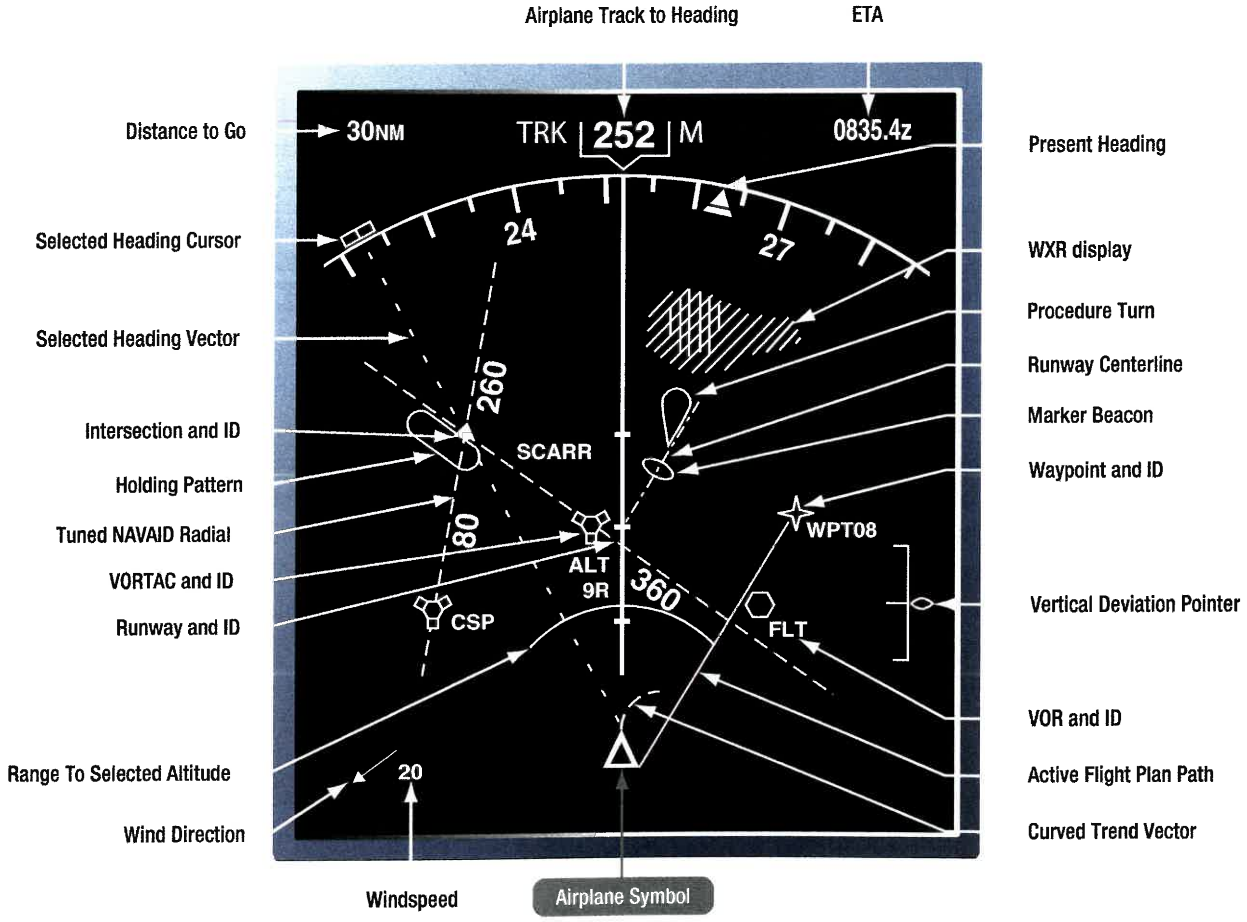


Figure 1-8. Navigation map display format.

performed by the Flight Engineer in three crew member cockpits. As previously shown in ***Figure 1-6***, the two EICAS displays on the B777 are located in the center instrument panel. The upper EICAS display shows engine performance data, such as pressure ratio, N1 rotor speed, exhaust gas temperature, total air temperature, thrust mode, etc., in addition to cabin pressure, flat/slat position, landing gear position, and crew status alerts. (***Figure 1-9***)

The EICAS engine display format mimics the round analog instruments, while also providing digital readouts of the parameters. EICAS improves situational awareness by allowing the crew to see systems operation in graphical format and alerting them to any failures or impending failures. For example, if low oil pressure is detected, the EICAS will provide an aural alert and show to the oil pressure page on a lower display with a red box outlining which engine has low oil pressure.

The Airbus ECAM system provides the crew with the following levels of warning along with detailed messages as to the nature of the problem and suggested courses of action.

- **Level 3**: An overspeed, fire, or stall condition will cause a repetitive chime aural warning with a bright red flashing light.
- **Level 2**. A system failure, but not a safety of flight issue, will result in a single chime aural warning and a steady amber light.

Figure 1-9. EICAS engine display format.

- **Level 1**: Failure leading to system degradation results only in an amber light.
- **Mode or System Status**. If everything is normal, a green light will illuminate.

The lower EICAS display is called a Multi-Function Display because it provides auxiliary information to the flight crew and maintenance crew. The MFD can be used as a secondary engine display, status display, communications display, maintenance page, or electronic checklist. The MFD formats also include synoptic displays that provide system status diagrams for the fuel, electrical, hydraulic, flight control, and environmental control systems, in addition to showing door and landing gear positions. On some aircraft, the MFD is also used to display images from the ground maneuvering camera system.

Figure 1-10 is a schematic diagram of an Engine Indication and Crew Alerting System with all its associated components. The display select panel allows the crew to choose which computer is actively supplying information. It also controls the display of secondary engine information and system status displays on the lower monitor.

EICAS has a unique feature that automatically records the parameters of a failure event to be regarded afterwards by maintenance personnel. Pilots that suspect a problem may be occurring during flight can press the event record button on the display select panel. This also records the parameters for that flight period to be studied later by maintenance. Hydraulic, electrical, environmental, performance, and Auxiliary Power Unit (APU) data are examples of what may be recorded. EICAS uses Built-In-Test Equipment (BITE) for systems and components. A maintenance control panel is included for technicians. When the aircraft is on the ground, push-button switches display information pertinent to various systems for analysis. (***Figure 1-11***)

This section contained an overview of a state-of-the-art aircraft cockpit with its Electronic Instrument System. The following section will discuss how digital data streams are formed and processed by aircraft computers and then sent over digital data buses to cockpit displays to provide essential information for the flight crew and maintenance crew.

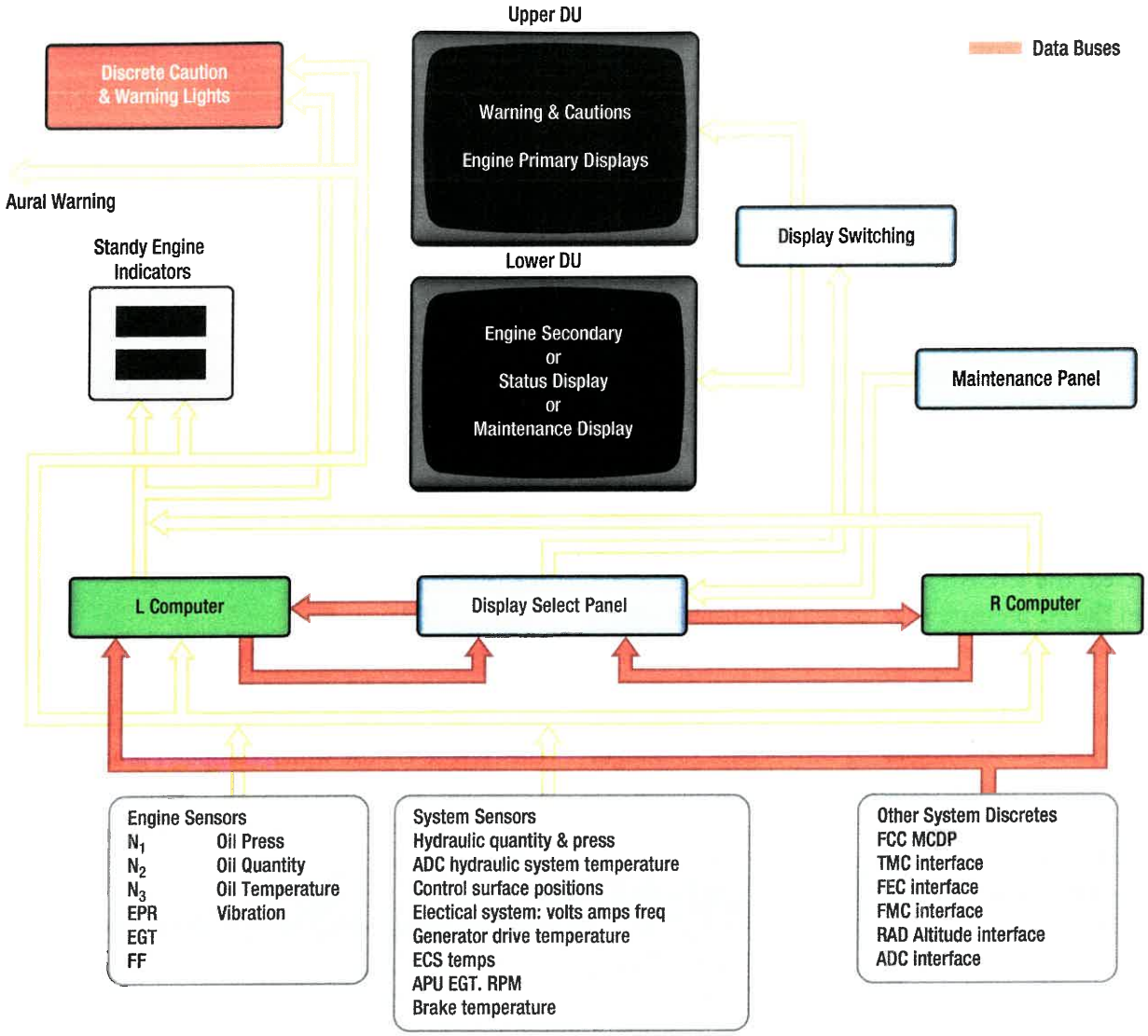


Figure 1-10. EICAS schematic diagram.

ELECTRONIC INSTRUMENT COMPUTING SYSTEMS

The Boeing 777 was the first commercial aircraft to make use of the Integrated Modular Avionics (IMA) concept in what Boeing calls its Airplane Information Management System (AIMS), the main computer for controlling the electronic instrument system. AIMS integrates multiple functions that require large quantities of data collection and processing. As shown in ***Figure 1-12***, AIMS provides the display processing and symbol generation for the two PFDs, two NDs, EICAS and MFD display units (DU).

AIMS interfaces with approximately 130 LRUs, sensors, switches and indicators through multiple data buses, in addition to analog and discrete (ON/OFF) signals, to permit the integration of information from a majority of aircraft systems in one place. The onboard maintenance system uses AIMS for the BITE computing function. Besides driving the six LCD electronic displays, AIMS accepts control inputs from the two EFIS control panels, two cursor control panels, two display switching panels, two instrument source select panels, a center display control panel, and display select panel. (***Figure 1-13***)

The Captain and First Officer display switching panels select the desired display format (PFD, NAV, MFD or EICAS) on the inboard display units. The normal modes for the inboard displays are either the Navigation (NAV) or Multi-Function Display (MFD) pages. The two cursor control devices are used to select and activate items on the MFDs, much like a mouse on a personal computer (PC).

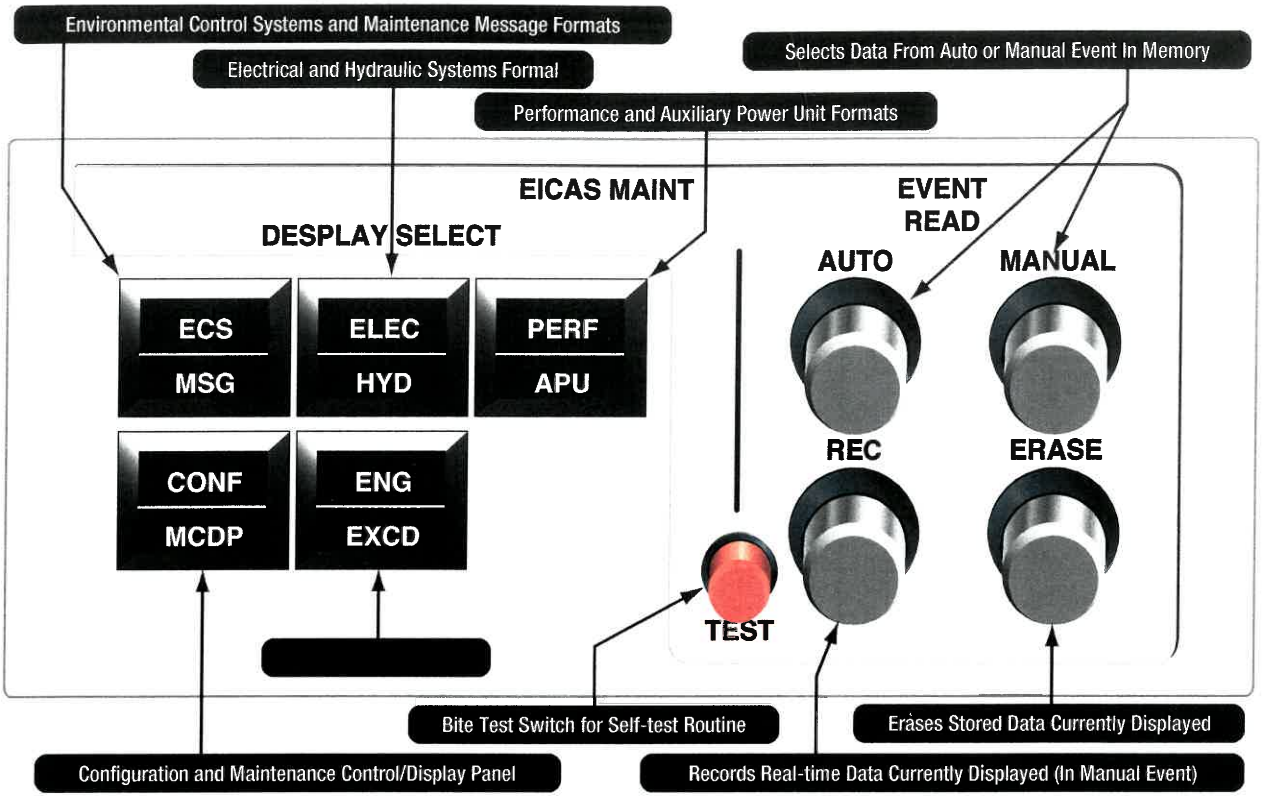


Figure 1-11. EICAS maintenance control panel.

The EFIS (Electronic Flight Instrumentation System) controls are used to select the desired source of the EFIS data. For the PFD (Primary Flight Display), the EFIS control panel selects the barometric altitude reference, radio altitude decision height, flight path vector and altitude reference. For the ND (Navigation Display), it selects the display mode format (map, plan, approach, or VOR navigation) and range, and turns on/off the VOR (VHF Omni-Range) and ADF (Automatic Direction Finder) pointers, Weather Radar (WXR) display, TCAS (Traffic Alert and Collision Avoidance System) display, and other navigation and surveillance inputs.

Electronic Instrument Computing Systems are triple redundant to allow for several automatic reversionary and manual override modes to switch out faulty Display Management Computers (DMC) if the event of a failure. ***Figure 1-14*** shows the architecture of the Airbus A330 Electronic Instrument System (EIS) in normal mode where DMC-1 is driving the Captain's EFIS PFD and ND, DMC-2 is driving the First Officer's EFIS PFD and ND, and DMC-3 is driving the ECAM (Electronic Centralized Aircraft Monitor) Engine/ Warning Display (E/WD) and System Display (SD). Note that the SD on the Airbus aircraft provides the same function as an MFD on Boeing aircraft.

In the event that an outboard display unit fails, the altitude, attitude, and airspeed information that was displayed on the PFD will automatically revert to being displayed on the inboard display unit since flying the aircraft always takes precedence over navigation. Likewise, if the top center DU fails, engine and warning information will revert to being displayed on the SD. ***Figure 1-15*** depicts how the system would reconfigure in the event of a multiple DMC failure. In this example, the EFIS computer fails in DMC-2 and both the EFIS and ECAM computers fail in DMC-3. In this case, the First Officer's EFIS would be driven by DMC-1 with the same display formats as the Captain, and the ECAM would run off of DMC-1 or DMC-2.

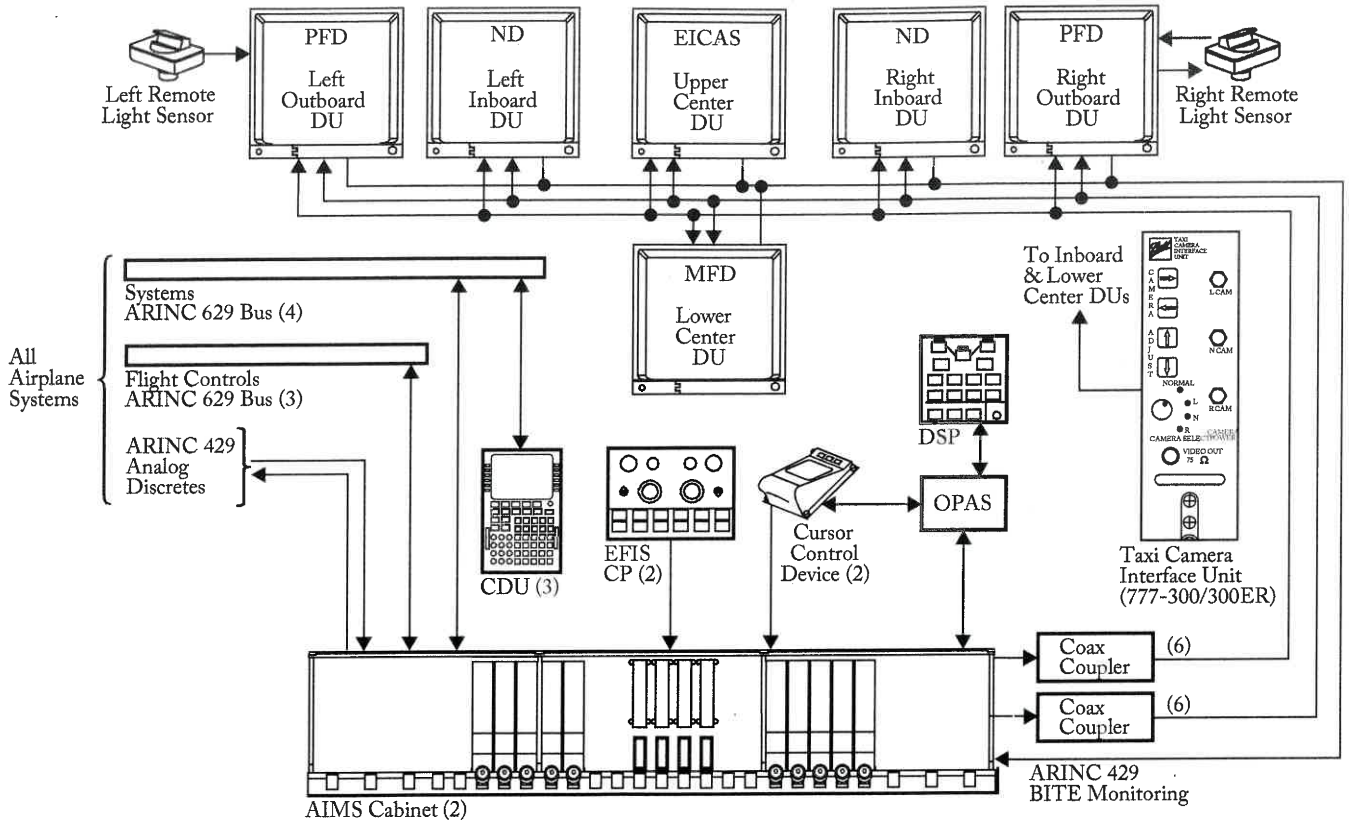


Figure 1-12. AIMS is the EIS computing system for the Boeing 777.

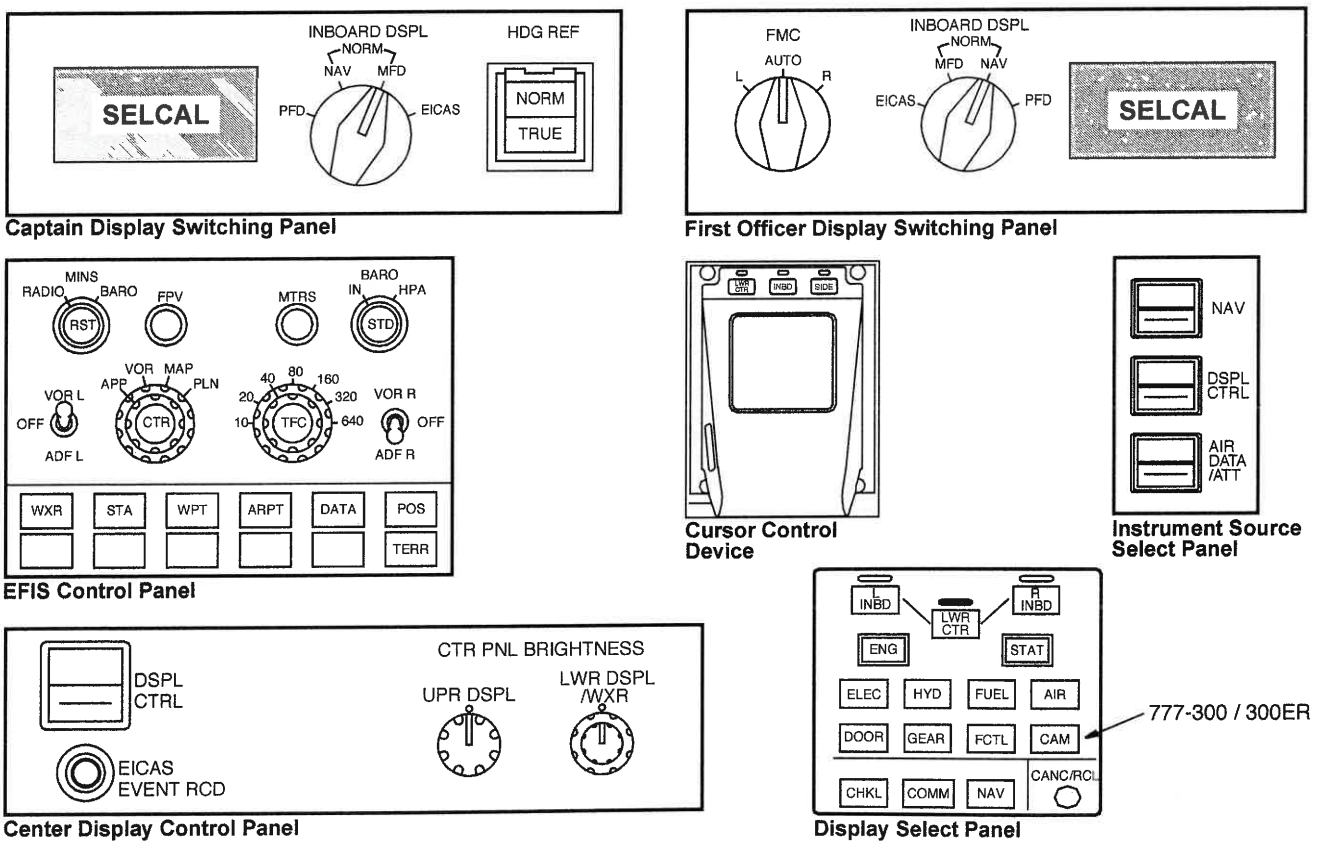


Figure 1-13. AIMS accepts control inputs from multiple display control panels.

RECONFIGURATION POSSIBILITIES - ARCHITECTURE

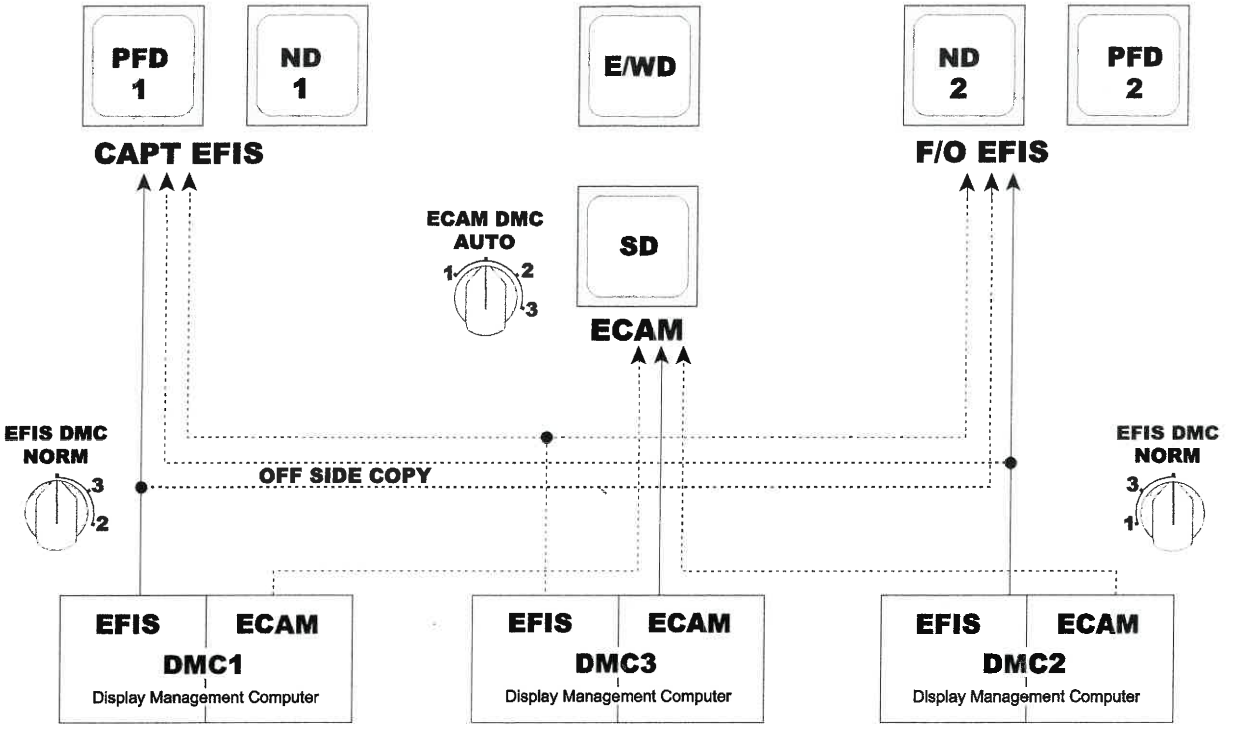


Figure 1-14. Airbus A330 EIS reconfiguration possibilities.

Reconfiguration - ECAM on DMC1 + F/O on EFIS DMC1

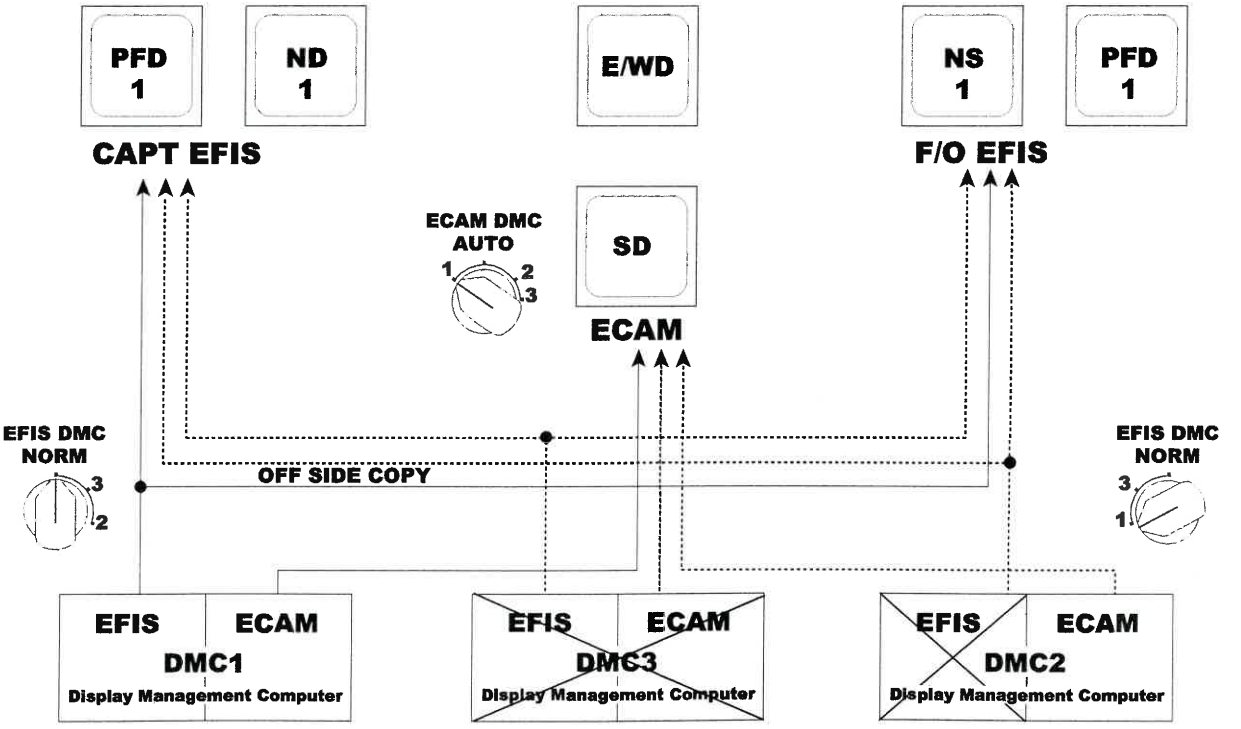


Figure 1-15. One of many reversionary modes in the event of multiple DMC failures.

Question: 1-1
What are the differences between analog and digital instruments?

Question: 1-2
What are the advantages of Liquid Crystal Displays (LCD) over Cathode Ray Tube (CRT) instruments used in "Glass Cockpits"?

Question: 1-3
What types of information does an Electronic Attitude Direction Indicator (EADI) and an Electronic Horizontal Situation Indicator (EHIS) provide to the flight crew?

Question: 1-4
What is the purpose of the Multi-Function Display (MFD)?

Question: 1-5
What information does a Primary Flight Display (PFD) provide?

Question: 1-6
What type of information is typically overlaid on the Navigation Display (ND)?

Question: 1-7
How information does the Engine Indication and Crew Alerting System (EICAS) provide to improve crew situational awareness?

Question: 1-8
What occurs when the flight crew pushes the "event" button on the EICAS Display Select Panel?

ANSWERS

Answer: 1-1
Analog instruments are typically mechanical or electro-mechanical devices, whereas digital instruments are driven by a digital data stream sent from a computer, called a Display Processor Unit or a Symbol Generator.

Answer: 1-2
Flat-panel LCDs are lighter than CRT displays, require less volume, and require less electrical power, thereby generating less cockpit heat.

Answer: 1-3
The EADI is an artificial horizon with lateral bars superimposed to display computer-generated pitch and bank steering commands from the Flight Director computer. The EHSI is similar to a heading indicator, except that it combines navigation commands from the VHF Omni-Range (VOR) or Global Positioning System (GPS) receivers which are used for en-route guidance, or from the Instrument Landing System (ILS), which is used for terminal guidance.

Answer: 1-4
The MFD is typically used to display weather radar information; however, it can also be used to display either flight information or navigational information in the event of an EADI or EHSI failure. In addition, the MFD can be used as a secondary engine display, status display, communications display, maintenance page, or electronic checklist. The MFD formats also include synoptic displays that provide system status diagrams for the fuel, electrical, hydraulic, flight control, and environmental control systems, in addition to showing door and landing gear positions.

Answer: 1-5
The PFD takes the place of the EADI and displays all the information critical to flight, including attitude, airspeed, barometric altitude, vertical speed, heading, flight modes, radio altitude, ILS data, and Traffic Alert and Collision Avoidance System (TCAS) resolution advisory.

Answer: 1-6
Some examples of information that is typically overlaid on the ND include weather information from either the onboard weather radar or ground based sensors, and digital maps showing pre-programmed routes and waypoints from the Flight Management System.

Answer: 1-7
The EICAS display shows engine performance data, such as pressure ratio, N1 rotor speed, exhaust gas temperature, total air temperature, thrust mode, etc., in addition to cabin pressure, flat/slat position, landing gear position, and crew status alerts. EICAS improves situational awareness by allowing the crew to see systems operation in graphical format and alerting them to any failures or impending failures.

Answer: 1-8
Pushing the event button records the parameters for that flight period to be studied later by maintenance. Hydraulic, electrical, environmental, performance, and Auxiliary Power Unit (APU) data are examples of what may be recorded.

DIGITAL TECHNIQUES ELECTRONIC INSTRUMENT SYSTEMS

NUMBERING SYSTEMS

SUB-MODULE 02

PART-66 SYLLABUS LEVELS

CERTIFICATION CATEGORY → B2

Sub-Module 02

NUMBERING SYSTEMS

Knowledge Requirements

5.2 - Numbering Systems		
	Numbering systems: binary, octal and hexadecimal; Demonstration of conversions between the decimal and binary, octal and hexadecimal systems and vice versa.	2

5.2 - NUMBERING SYSTEMS

DECIMAL

Numbers are used to describe the quantity of something. A numbering system is a written system for expressing numbers as symbols. All numbering systems have bases to understand how the numbering system works. For example, the symbol "10" could mean "ten" in decimal form (base-10) or it could mean "two" in binary form (base-2). To differentiate between them, express a decimal as 10 $base_{10}$ or 10_{10}.

The most common numbering system that used in everyday life is the decimal system. The prefix in the word "decimal" is a Latin root for the word "ten". Thus, the decimal system uses ten different symbols (0, 1, 2, 3, 4, 5, 6, 7, 8, and 9) and is referred to as a base-10 numbering system. To represent a number higher than 9, go to the next digit placement, such that 10 means zero units of one and one unit of ten. At the last symbol, a new placement is created to the left and counted up, so that 100 appears after 99, and so on. Each additional placement is an additional power of 10. Knowing this will help in understanding the other bases.

BINARY

The binary number system has only two symbols: 0 and 1. The prefix in the word "binary" is a Latin root for the word "two", and as such, is referred to as a base-2 numbering system. The use of the binary numbering system is based on the fact that switches or valves have two states: OPEN or CLOSED (ON or OFF).

Primary uses of the binary number system include computer architecture and digital electronics. In computers, information is stored as a series of 0's and 1's, forming strings of binary numbers known as machine language. Similarly, the binary number system is used in digital electronics because the two basic conditions of electricity, ON and OFF, can represent the two digits of the binary number system. When a switch is ON, it represents the digit 1, and when it is OFF, it represents the digit 0.

Millions and even billions of tiny switches are arranged so that digital devices can perform the functions they do with a binary number system. It is easy to recognize a binary number when written because it only uses 1's and 0's. To ensure it is not mistaken for another number system expression, a binary number system numeral may be written with a prefix or suffix that indicates it is binary. Binary number system identifiers are shown in the following example. There are others. The value of all of the binary numbers shown in this example is the same (11 in the decimal number system).

1011_2, 1011 $base_2$, bin 1011, 0b1011, 1011b

When reading or pronouncing a binary number, it is common to simply say "1" or "0" moving from left to right until all the digits are pronounced.

To read 1011_2, say, "one, zero, one, one"

PLACE VALUES

As stated previously, the decimal number system used in everyday life is a base-10 system. There are 10 symbols available for use as place value holders; 0, 1, 2, 3, 4, 5, 6, 7, 8, and 9. When positioned in a number, they are also positioned to represent a place value. If 9 is exceeded, the place value resets to 0 and a 1 must be placed in the next place value column to the left. ***Figure 2-1*** illustrates the decimal number system place values. They are derived by sequentially raising 10 to a higher power moving from right to left. Thus, each position has a value 10 times that of the position to its right.

The binary number system is a base-2 system. There are 2 digits available for use as place value holders; 0 and 1. Each place value in the binary number system represents 2 raised to a sequentially higher power from right to left. This is similar to the decimal system used in everyday life.

DECIMAL PLACE VALUE CHART

10^7	10^6	10^5	10^4	10^3	10^2	10^1	10^0
= 10 000 000	= 1 000 000	= 100 000	= 10 000	= 1 000	= 100	= 10	= 1

Figure 2-1. Place values of the decimal number system.

BINARY PLACE VALUE CHART

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
= 128	= 64	= 32	= 16	= 8	= 4	= 2	= 1

Figure 2-2. Derivation of the place values of the binary number system.

Figure 2-2 illustrates the place values of the binary number system. It shows to what power 2 is raised to establish value and the decimal number system equivalent of each place. Each place value position has a value 2 times that of the position to its right.

Remember, when writing binary numbers and placing digits in positions of place value, the only digits available are 0 and 1. To exceed 1, the place value is reset to 0 and a 1 is placed in the next place value column to the left. Place values are used to convert our everyday decimal numbers to binary numbers.

Figure 2-3 illustrates how binary numbers are formed by placing a 1 or a 0 in the binary place value positions. Binary digits are called "bits". The Least Significant Bit (LSB) is the bit with the smallest weight. The LSB on the far right of the binary place value position table is 2^0, which equals 1. In this last column, alternate every other time going down the column inserting 1s and 0s. Likewise, the next LSB is 2^1, or 2, which means alternate every 2 times down the column inserting 1s and 0s, and so forth.

	BINARY PLACE VALUE POSITIONS			
DECIMAL	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Figure 2-3. Binary value place positions.

The Most Significant Bit (MSB) is the bit with the largest weight. The MSB is on the far left side of the binary place value position table. Here the bits alternate every 8 times between 1s and 0s. Together all four bits across each row form the binary equivalent of the decimal number shown in the far left column.

BINARY NUMBER SYSTEM CONVERSION

Each binary number column has a decimal value. To convert from decimal to binary, find the binary column that has the largest value but is equal to or smaller than the decimal number being converted. Place a 1 in that column and subtract the column value from the decimal number being converted. Look at the difference. Place a 1 in the column that has the largest value but is equal to or smaller than the decimal number difference of what was just subtracted. Now subtract this column value from the difference of the decimal number being converted and the previous column difference. If a column is not used, place a zero in it. Continue this operation until all of the binary place value columns with 1's, when added together, have the same value as the decimal number being converted. Write the number in binary form including a 1 or a 0 for each column.

Example: Convert the decimal number 100_{10} to a binary number. Use the binary place value chart in ***Figure 2-4*** to assist in remembering the decimal equivalent value for each binary place value holder. The largest decimal number system value in a binary number system place holder that is less than or equal to 100 is 64. Thus, a 1 is paced in the 64 column (2^6) of the binary place value chart. Subtract 64 from 100 for a difference of 36.

The binary place value holder that is less than or equal to 36 is 32. Place a 1 in the 32 column (2^5) of the binary place value chart. Subtract 32 from 36 for a difference of 4. The binary place value holder that is less than or equal to 4 is 4. Place a 1 in the 4 column (2^2) of the binary place value chart. Subtract 4 from 4 for a difference of 0. Since there is nothing left to be converted, place a 0 in all place value columns that do not contain a 1. Write the number using all the 1's and 0's recorded in the chart from right to left; $1100100_2 = 100_{10}$

To convert a binary number to a decimal number, simply add the column values of the binary place holders with a 1.

Example: Convert the binary number 10010111 to a decimal number. From left to right, the base-2 values represent by each 1 in this binary number are added together: 128 + 16 + 4 + 2 + 1 = 151. $10010111_2 = 151_{10}$.

As can be seen, a binary number is typically much longer that its decimal equivalent. However, modern circuits have very fast switching speeds so that the length of binary numbers can be tolerated. This is especially true because of the reliability that is gained from a system that is built from components that are either 1 (ON) or 0 (OFF), that is, either have voltage or do not have voltage.

OCTAL

The binary numbering system requires many bits to represent relatively small numbers. In the preceding example, it required 8 binary bits (10010111) to represent a 3-digit decimal (151). As such, analyzing the numerical states of digital logic using the binary numbering system can become quite tedious for computer programmers developing machine language code. For this reason, place-weighted numbering systems, such as octal, were developed. The prefix in the word "octal" is a Latin root for the word "eight", and as such, it is referred to as a base-8 numbering system. Octal has 8 symbols available

DECIMAL NUMBER	2^7 = 128	2^6 = 64	2^5 = 32	2^4 = 16	2^3 = 8	2^2 = 4	2^1 = 2	2^0 = 1
1								1
2							1	0
3							1	1
5						1	0	1
8					1	0	0	0
20				1	0	1	0	0
35			1	0	0	0	1	1
96		1	1	0	0	0	0	0
100		1	1	0	0	1	0	0
200	1	1	0	0	1	0	0	0
255	1	1	1	1	1	1	1	1

Figure 2-4. Use of binary number system place values to write various decimal numbers in binary (base2).

as place value holders (0, 1, 2, 3, 4, 5, 6, and 7). As shown in ***Figure 2-5***, each place weight differs from the one next to it by a factor of 8, instead of only by a factor of 2 as in the binary system.

OCTAL PLACE VALUE CHART

To convert an octal number to a decimal, one must multiply the value of the power of 8 depending on where the digit falls on the above octal place value chart.

Example: Convert octal number 42 to a decimal. The least significant digit of 2 is multiplied by 8^0, which is 1, and the next digit of 4 is multiplied by 8^1, which is 8. The results are then added as shown below.

$2 \times 1 = 2,\ 4 \times 8 = 32,\ 2 + 32 = 34$

OCTAL NUMBER SYSTEM CONVERSION

Octal numerals can be made from binary numerals by grouping consecutive binary digits into groups of three. To convert a decimal to an octal number, begin by converting the decimal to a binary number. Then separate the binary number into groups of 3 digits starting from the right. If needed, add implied zeros to the left of the number to form complete groups of 3 digits each. Next, convert each group of 3 digits to an octal value using ***Figure 2-6***.

OCTAL PLACE VALUE CHART

8^7	8^6	8^5	8^4	8^3	8^2	8^1	8^0
2 097 152	262 144	32 768	4 096	512	64	8	1

Figure 2-5. Derivation of the place values of the octal number system.

DECIMAL	BINARY	OCTAL	HEX
0	00000000	000	0
1	00000001	001	1
2	00000010	002	2
3	00000011	003	3
4	00000100	004	4
5	00000101	005	5
6	00000110	006	6
7	00000111	007	7
8	00001000	010	8
9	00001001	011	9
10	00001010	012	A
11	00001011	013	B
12	00001100	014	C
13	00001101	015	D
14	00001110	016	E
15	00001111	017	F
16	00010000	020	10
17	00010001	021	11
18	00010010	022	12
19	00010011	023	13
20	00010100	024	14
21	00010101	025	15
22	00010110	026	16
23	00010111	027	17
24	00011000	030	18
25	00011001	031	19
26	00011010	032	1A
27	00011011	033	1B
28	00011100	034	1C
29	00011101	035	1D
30	00011110	036	1E
31	00011111	037	1F
32	00100000	040	20
33	00100001	041	21
34	00100010	042	22
35	00100011	043	23
36	00100100	044	24
37	00100101	045	25
38	00100110	046	26
39	00100111	047	27
40	00101000	050	28
41	00101001	051	29
42	00101010	052	2A
43	00101011	053	2B
44	00101100	054	2C
45	00101101	055	2D
46	00101110	056	2E
47	00101111	057	2F
48	00110000	060	30
49	00110001	061	31
50	00110010	062	32
51	00110011	063	33
52	00110100	064	34
53	00110101	065	35
54	00110110	066	36
55	00110111	067	37
56	00111000	070	38
57	00111001	071	39
58	00111010	072	3A
59	00111011	073	3B
60	00111100	074	3C
61	00111101	075	3D
62	00111110	076	3E
63	00111111	077	3F
64	01000000	100	40
65	01000001	101	41
66	01000010	102	42
67	01000011	103	43
68	01000100	104	44
69	01000101	105	45
70	01000110	106	46
71	01000111	107	47
72	01001000	110	48
73	01001001	111	49
74	01001010	112	4A
75	01001011	113	4B
76	01001100	114	4C
77	01001101	115	4D
78	01001110	116	4E
79	01001111	117	4F
80	01010000	120	50
81	01010001	121	51
82	01010010	122	52
83	01010011	123	53
84	01010100	124	54
85	01010101	125	55
86	01010110	126	56
87	01010111	127	57
88	01011000	130	58
89	01011001	131	59
90	01011010	132	5A
91	01011011	133	5B
92	01011100	134	5C
93	01011101	135	5D
94	01011110	136	5E
95	01011111	137	5F
96	01100000	140	60
97	01100001	141	61
98	01100010	142	62
99	01100011	143	63
100	01100100	144	64

Figure 2-6. Binary to octal and hexadecimal conversion table.

HEXADECIMAL PLACE VALUE CHART

16^7	16^6	16^5	16^4	16^3	16^2	16^1	16^0
259 435 456	16 777 216	1 048 576	65 536	4 096	256	16	1

Figure 2-7. Derivation of the place values of the hexadecimal number system.

Example: Convert the decimal number 100_{10} to an octal number by first converting it to its binary number of 001100100. Break the binary number into groups of three and convert.
001 = 1, 100 = 4, 100 = 4, Octal number = 144c

So as not to confuse an octal number of 144 with the decimal number of 100, any of the following conventions may be used either before or after the octal number.

144_8 144base8 oct 144 0c144 144c

HEXADECIMAL

Another place-weighted numbering system is hexadecimal with a base of 16. Each hexadecimal digit represents four binary digits (bits) and there are eight bits in each byte. Hexadecimal notation is more popular because binary bit grouping in computing and digital electronics are in multiples of eight (8, 16, 32, 64, and 128 bit). Hexadecimal symbols include normal decimal symbols of 0, 1, 2, 3, 4, 5, 6, 7, 8, and 9, plus six alphabetical characters of A, B, C, D, E, and F. The hexadecimal place value chart is shown in ***Figure 2-7***. Similar to the octal notation, each place weight differs from the one next to it, but by a factor of 16 (instead of 8), thereby reducing the number of bits in half to provide the same amount of information.

HEXADECIMAL PLACE VALUE CHART

To convert a hexadecimal (hex) number to a decimal, one must multiply the value of the power of 16 depending on where the digit falls on the above hexadecimal place value chart.

Example: Convert hex symbol 1A to a decimal. The least significant digit of A(10) is multiplied by 16^0, which is 10, and the next digit of 1 is multiplied by 16^1, which is 16. The results are then added as shown below.
$10 \times 1 = 10,\ 1 \times 16 = 16,\ 10 + 16 = 26$

So as not to confuse the hex number, of say 10, with the decimal number of 16, any of the following conventions may be used either before or after the hex number.

1016 10base16 hex10 0×10 10×

HEXADECIMAL NUMBER SYSTEM CONVERSION

Hex numerals can be made from binary numerals by placing consecutive binary digits into groupings of 4, instead of 3 as with octal numbers. To convert a decimal to a hex number, begin by converting the decimal to a binary number. Then separate the binary number into groups of 4 digits starting from the right. Again, add implied zeros to the left of the number to form complete groups of 4 digits each. Next, convert each group of 4 digits to a hexadecimal value using ***Figure 2-6***.

Example: Convert the decimal number 100_{10} to a hex number by first converting it to its binary number of 01100100. Break the binary number into groups of four starting from the right and convert.
0110 = 6, 0100 = 4, Hex number = 64×

To summarize, the "native language" of digital electronics, referred to as machine language, is binary. Octal and hexadecimal are more efficient variations of binary for programming since octal and hexadecimal are based on powers of 8 and 16, respectively, which are even multiples of the binary's base-2. This Sub-Module demonstrated how binary digits are grouped together and directly converted to or from their respective octal or hexadecimal numbers. It is important to understand that all digital devices, such as computers, will operate only off of binary digits known as bits.

BINARY-CODED DECIMALS

Computers instructions are formed by groupings binary digits to form words. A series of four binary digits will form a 4-bit word. These 4-bit words are represented by Binary-Coded Decimals (BCD). As shown in ***Figure 2-3***, binary 1000 represents decimal 8 and binary 0010 represents decimal 2. BCD coding uses the binary equivalent of the decimal number; however, BCD coding and binary numbers are not the same.

A BCD number must be between decimal number 0 and 9 since each BCD number is expressed in units, tens, hundreds, thousands, etc. For example, the binary number equivalent of decimal 82 is 01010010. However, the BCD expression would be two 4-bit words consisting of 1000 representing number 8 and 0010 representing number 2 as two separate decimals.

Example: Convert the decimal number 264_{10} to a BCD number by first separating each decimal number in to its place value and then converting each decimal in to 4-bit BCD words.

2 = 0010, 6 = 0110, 4 = 0100

ASCII

The American Standard Code for Information Interchange (ASCII) was developed as a character encoding scheme for teletype and computer keyboards. As such, it is based on the English alphabet and encodes 128 specified characters into 7-bit binary numbers as shown in ***Figure 2-8***. For example, entering the letter "A" on a keyboard would output binary number 1000001 to the input of a computer as an instruction.

DEC	HEX	OCT	BIN	CHAR	DEC	HEX	OCT	BIN	CHAR	DEC	HEX	OCT	BIN	CHAR
0	0×00	000	0000000	NUL	54	0×36	066	0110110	6	108	0×6C	154	1101100	l
1	0×01	001	0000001	SOH	55	0×37	067	0110111	7	109	0×6D	155	1101101	m
2	0×02	002	0000010	STX	56	0×38	070	0111000	8	110	0×6E	156	1101110	n
3	0×03	003	0000011	ETX	57	0×39	071	0111001	9	111	0×6F	157	1101111	o
4	0×04	004	0000100	EOT	58	0×3A	072	0111010	:	112	0×70	160	1110000	p
5	0×05	005	0000101	ENQ	59	0×3B	073	0111011	;	113	0×71	161	1110001	q
6	0×06	006	0000110	ACK	60	0×3C	074	0111100	<	114	0×72	162	1110010	r
7	0×07	007	0000111	BEL	61	0×3D	075	0111101	=	115	0×73	163	1110011	s
8	0×08	010	0001000	BS	62	0×3E	076	0111110	>	116	0×74	164	1110100	t
9	0×09	011	0001001	TAB	63	0×3F	077	0111111	?	117	0×75	165	1110101	u
10	0×0A	012	0001010	LF	64	0×40	100	1000000	@	118	0×76	166	1110110	v
11	0×0B	013	0001011	VT	65	0×41	101	1000001	A	119	0×77	167	1110111	w
12	0×0C	014	0001100	FF	66	0×42	102	1000010	B	120	0×78	170	1111000	x
13	0×0D	015	0001101	CR	67	0×43	103	1000011	C	121	0×79	171	1111001	y
14	0×0E	016	0001110	SO	68	0×44	104	1000100	D	122	0×7A	172	1111010	z
15	0×0F	017	0001111	SI	69	0×45	105	1000101	E	123	0×7B	173	1111011	{
16	0×10	020	0010000	DLE	70	0×46	106	1000110	F	124	0×7C	174	1111100	|
17	0×11	021	0010001	DC1	71	0×47	107	1000111	G	125	0×7D	175	1111101	}
18	0×12	022	0010010	DC2	72	0×48	110	1001000	H	126	0×7E	176	1111110	~
19	0×13	023	0010011	DC3	73	0×49	111	1001001	I	127	0×7F	177	1111111	DEL
20	0×14	024	0010100	DC4	74	0×4A	112	1001010	J					
21	0×15	025	0010101	NAK	75	0×4B	113	1001011	K					
22	0×16	026	0010110	SYN	76	0×4C	114	1001100	L					
23	0×17	027	0010111	ETB	77	0×4D	115	1001101	M					
24	0×18	030	0011000	CAN	78	0×4E	116	1001110	N					
25	0×19	031	0011001	EM	79	0×4F	117	1001111	O					
26	0×1A	032	0011010	SUB	80	0×50	120	1010000	P					
27	0×1B	033	0011011	ESC	81	0×51	121	1010001	Q					
28	0×1C	034	0011100	FS	82	0×52	122	1010010	R					
29	0×1D	035	0011101	GS	83	0×53	123	1010011	S					
30	0×1E	036	0011110	RS	84	0×54	124	1010100	T					
31	0×1F	037	0011111	US	85	0×55	125	1010101	U					
32	0×20	040	0100000	space	86	0×56	126	1010110	V					
33	0×21	041	0100001	!	87	0×57	127	1010111	W					
34	0×22	042	0100010	"	88	0×58	130	1011000	X					
35	0×23	043	0100011	#	89	0×59	131	1011001	Y					
36	0×24	044	0100100	$	90	0×5A	132	1011010	Z					
37	0×25	045	0100101	%	91	0×5B	133	1011011	[					
38	0×26	046	0100110	&	92	0×5C	134	1011100	\					
39	0×27	047	0100111	'	93	0×5D	135	1011101	]					
40	0×28	050	0101000	(	94	0×5E	136	1011110	^					
41	0×29	051	0101001	)	95	0×5F	137	1011111	_					
42	0×2A	052	0101010	*	96	0×60	140	1100000	'					
43	0×2B	053	0101011	+	97	0×61	141	1100001	a					
44	0×2C	054	0101100	,	98	0×62	142	1100010	b					
45	0×2D	055	0101101	-	99	0×63	143	1100011	c					
46	0×2E	056	0101110	.	100	0×64	144	1100100	d					
47	0×2F	057	0101111	/	101	0×65	145	1100101	e					
48	0×30	060	0110000	0	102	0×66	146	1100110	f					
49	0×31	061	0110001	1	103	0×67	147	1100111	g					
50	0×32	062	0110010	2	104	0×68	150	1101000	h					
51	0×33	063	0110011	3	105	0×69	151	1101001	i					
52	0×34	064	0110100	4	106	0×6A	152	1101010	j					
53	0×35	065	0110101	5	107	0×6B	153	1101011	k					

Figure 2-8. ASCII conversion chart.

Question: 2-1
Explain the decimal numbering system. How many symbols and what is its power?

Question: 2-2
Why is the binary numbering system used in digital electronics?

Question: 2-3
When writing binary numbers and placing digits in positions of place value, what occurs when a place value exceeds 1?

Question: 2-4
Where is the Least Significant Bit (LSB) located on the binary place value table?

Question: 2-5
Explain how to convert a decimal number to a binary number.

Question: 2-6
Why are place-weighted numbering systems, such as octal and hexadecimal, used?

Question: 2-7
Convert the decimal number 100_{10} to an octal number.

Question: 2-8
Convert hex symbol 1A to a decimal.

ANSWERS

Answer: 2-1
The decimal system uses ten different symbols (0, 1, 2, 3, 4, 5, 6, 7, 8, and 9) and is referred to as a base-10 numbering system since each additional placement is an additional power of 10.

Answer: 2-2
The binary number system is used in digital electronics because the two basic conditions of electricity, ON and OFF, can represent the two digits of the binary number system. When a switch is ON, it represents the digit 1, and when it is OFF, it represents the digit 0.

Answer: 2-3
The only digits available are 0 and 1. To exceed 1, the place value is reset to 0 and a 1 is placed in the next place value column to the left.

Answer: 2-4
The LSB is always located on the far right of the binary place value table at 20.

Answer: 2-5
To convert from decimal to binary, find the binary column that has the largest value but is equal to or smaller than the decimal number being converted. Place a 1 in that column and subtract the column value from the decimal number being converted. Look at the difference. Place a 1 in the column that has the largest value but is equal to or smaller than the decimal number difference of what was just subtracted. Now subtract this column value from the difference of the decimal number being converted and the previous column difference. If a column is not used, place a zero in it. Continue this operation until all of the binary place value columns with 1's, when added together, have the same value as the decimal number being converted. Write the number in binary form including a 1 or a 0 for each column.

Answer: 2-6
The binary numbering system requires many bits to represent relatively small numbers. For example, 8 binary bits (10010111) are required to represent a 3-digit decimal (151). As such, analyzing the numerical states of digital logic using the binary numbering system can become quite tedious for computer programmers developing machine language code.

Answer: 2-7
First convert 100_{10} to its binary number of 01100100. Then break the binary number into groups of three and convert as shown below:

001 = 1, 100 = 4, 100 = 4
Octal number = 144c

Answer: 2-8
The least significant digit of A is multiplied by 160, which is 10, and the next digit of 1 is multiplied by 161, which is 16. The results are then added as shown below.

$10 \times 1 = 10$, $1 \times 16 = 16$, $10 + 16 = 26$

PART-66 SYLLABUS LEVELS

CERTIFICATION CATEGORY → B2

Sub-Module 03

DATA CONVERSION

Knowledge Requirements

5.3 - Data Conversion

Analogue Data, Digital Data; 2

Operation and application of analogue to digital, and digital to analogue converters, inputs and outputs, limitations of various types.

ANALOG DATA

Analog and digital signals can both contain the same useful information. For example, an analog watch with hands pointing to numbers on a dial tells the time just as well as a LCD watch that displays digital numbers. The advantage of the analog watch is that is that it tells time in relative terms, such as ¼ past the 11th hour; whereas the digital watch tells time in discrete units, such as 11:15 am. Many cockpit instruments display both analog and digital formats.

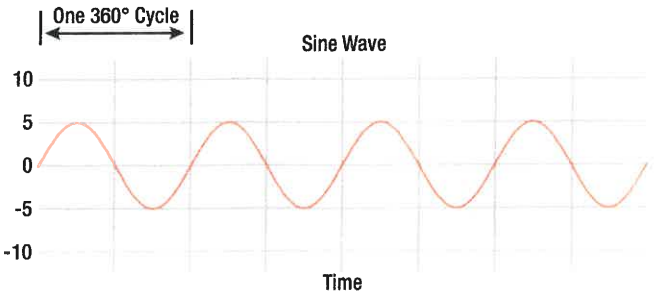


Figure 3-1. AC analog signal (sine wave).

Analog circuits are different from digital circuits in that they do not have two set values, such as 0 volts representing "OFF" and 5 volts representing "ON". Instead, analog circuits will vary continuously in both time and value from high to low. AC (alternating current) analog signals can be bipolar in that they have both positive and negative limits as seen in an AC sine wave. ***Figure 3-1*** illustrates the sine wave output of an AC synchronous transmitter that varies in value (amplitude) from 0 volts to its +5 volt limit and returns to 0 volts before moving to its -5 volt limit and then back to 0 volts in one time cycle. DC (direct current) analog signals are unipolar in that they will have 0 volts as one of its limits with some level of either positive or negative voltage defining its other analog signal voltage range limit, but will never alternate between positive and negative voltages.

Analog signals have the advantage in that they can represent any functional quantity, such as time, temperature, pressure, etc., by outputting an equivalent functional quantity of voltage or current. Prime examples are analog fuel quantity and oil pressure synchro systems. By locating the transmitter of a synchro system remotely, fluid pressure can be directed into it without the necessity of running tubing through to the cockpit.

Inside the transmitter, the motion of a pressure bellows can be geared to the transmitter rotor in such a way as to make the rotor turn. (***Figure 3-2***) As in all synchros, the transmitter rotor turns proportional to the pressure sensed, which vary the voltages set up in the windings of the synchro stator. These voltages are transmitted to the indicator coils that develop the magnetic field that positions the pointer.

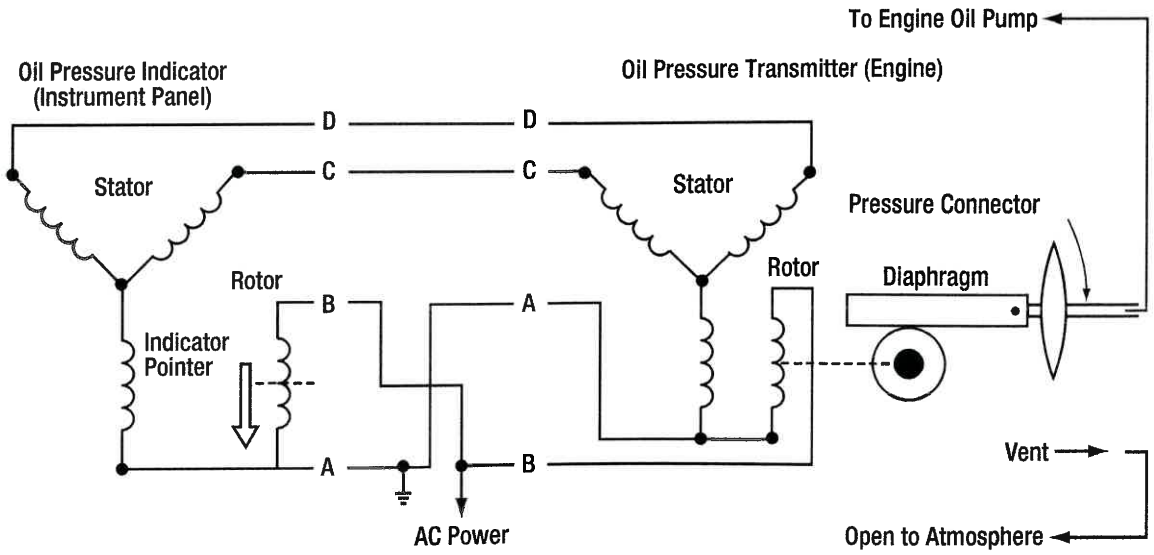


Figure 3-2. Analog synchro instrument system.

Aircraft with digital instrumentation make use of pressure sensitive solid-state sensors that output digital signals for collection and processing by aircraft computers. Others may retain their analog sensors, but may forward this information through an analog-to-digital (A/D) converter for a computer to process and present the digital information to cockpit displays.

DIGITAL DATA

Analog circuits and devices vary continuously in both time and value from high to low; however, digital data are discrete and discontinuous representations of information. Digital signals are different from analog signals in that there are only two (binary) levels of voltage: high for "ON" and low for "OFF". These two different voltage levels are put into a sequence of digital numbers to describe the value being transmitted. As stated in the previous Sub-Module, the binary number system is used in digital electronics because the two basic conditions of electricity, ON and OFF, can represent the two digits of the binary number system. When a switch is ON, it represents the digit 1, and when it is OFF, it represents the digit 0. Digital circuits will be discussed later in *Sub-Module 05*.

ANALOG TO DIGITAL CONVERSION

As shown in ***Figure 3-3***, an Analog-to-Digital Converter (ADC) is a device that converts a continuous input voltage to a digital data stream that represents the amplitude of the input analog signal. As such, the ADC performs conversions periodically by sampling and quantizing the input signal over a very short period of time. The result is a sequence of digital numbers that have been converted from continuous time and amplitude analog signals to discrete time and amplitude digital signals.

To begin the A/D data conversion process, the voltage range is divided into 2^n equal bins and then sampled continuously at uniform intervals controlled by a clock timing signal. The value that is sampled is held until the next sample is taken. The ADC generates binary numbers that represents each voltage level sampled.

If the voltage is divided into 2^1 bins it will generate 2 bits per sample. As shown in ***Figure 3-4***, the first sample generates binary output 01 to represent 1 volt measured at the first interval, and the second sample results in a binary output of 10 which represents 2 volts at the second interval, and so on.

Figure 3-3. Symbol for an analog to digital converter.

Clearly, the digital representation of the analog waveform shown in ***Figure 3-4*** is a distorted version of the original analog signal, although the basic similarity of the two can be discerned. Errors are produced by dividing the voltage range into bins that implies conversion back to the original analog signal will produce the exact same values. Quantization error can be reduced by generating more bits per sample, with each bit occupying less of the overall voltage range. For example, a 4-bit ADC will sample 2^4 or 16 voltage bands, which is its decimal equivalent value of dynamic range. Dynamic range is the ratio of the largest input that can be converted to the smallest step size.

For example, a 4-bit ADC with an input of 0 to 5 volts has a quantization step size of 5 volts / 16 bands = 0.3125. Therefore, the dynamic range is calculated to be 5 / 0.3125 = 16.

Resolution refers to the number of quantization levels or bands that an ADC can sample. For example, an ADC that can determine which of 16 levels that an input signal lies would be said to have a 4-bit resolution. The resolution of the ADC, determined by the number of binary bits in the digital output, is the value of the smallest quantizing step size. Based on this, a 4-bit ADC has a quantizing accuracy of +/- 3.1%, and a

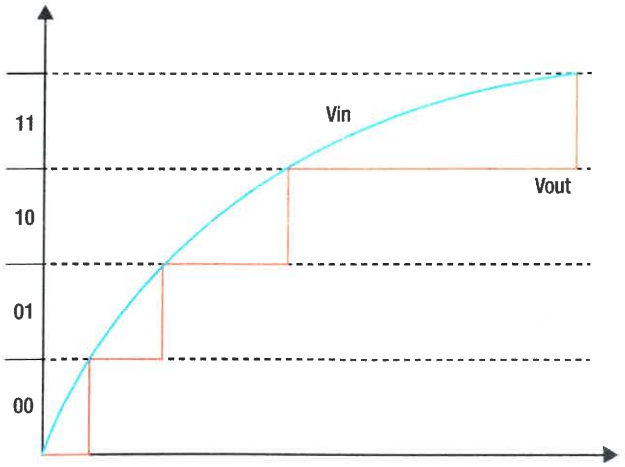


Figure 3-4. Analog-to-digital conversion by sampling and quantizing.

14-bit ADC would have a quantizing accuracy of +/- 0.006%. Resolution and the speed of conversion (also called latency) are the two most important operational parameters used in selecting ADCs. Latency is the interval of time between when an analog signal is sampled and when the associated digital code appears at the output. Note that the conversion time is not necessarily the reciprocal of the sampling rate.

The fastest type of ADC is the direct comparison converter (***Figure 3-5***), where by each reference voltage used in the comparison is assigned a digital value. The analog voltage (Vin) to be sampled appears at the input of all 7 high-gain differential operational amplifiers (op-amps). Each op-amp compares the analog input voltage with the fixed reference voltages (Vref) that are present at the remaining op-amp inputs. The resister ladder network divides the reference voltage range into 7 different voltage bins for sampling and quantization. The threshold detector in each op-amp drives the encoding logic that detects the highest reference that is exceeded. The ADC encoder then uses this information to produce a 3-bit binary output.

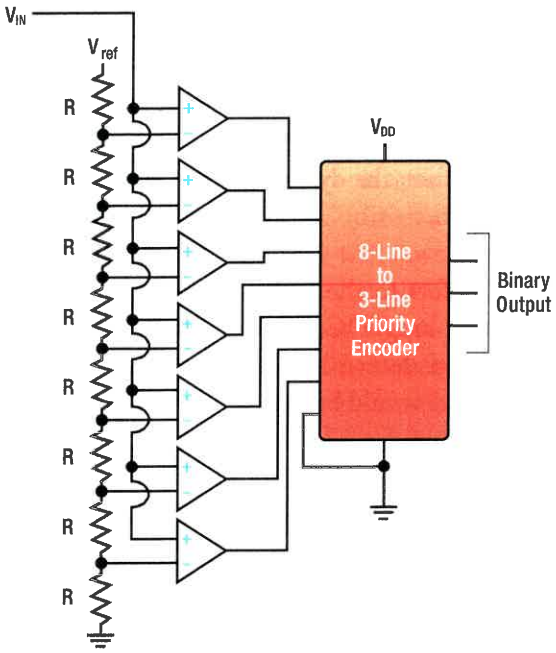


Figure 3-5. Direct comparison ADC circuit.

The direct comparison circuit may be the fastest ADC; however, its circuitry becomes quite large for outputs of more than 3 or 4 bits. In this case, integrating ADC are used, as shown in ***Figure 3-6***. This type of ADC uses a digital counter to count the time it takes for a reference voltage (VDAC) to integrate a charge on a capacitor to the same value as the analog input voltage. A reference ramp is generated by a clock timing signal turning on the analog input voltage to charge the integrating capacitor. The counter counts the clock pulses until the op-amp comparator indicates that the ramp has reached the analog input voltage level. At that point, the number of clock pulses counted is the digital equivalent of the analog voltage input.

DIGITAL TO ANALOG CONVERSION

Digital-to-Analog Converters (DACs) are found in everyday use. For example, digital information stored on Digital Video Discs (DVDs) and Compact Disc (CDs) use DACs to convert digital data streams to analog music and video signals. Digital-to-analog is the reverse of the above A/D conversion process such that each binary number is converted back into nominal levels by reconstructing the original waveform.

As shown in ***Figure 3-7***, a DAC is a device that reconstructs finite-precision time series data in to a continuously varying signal, which theoretically can have an infinite number of states. In simple terms, it takes binary numbers, or combination of binary numbers, and changes them into corresponding voltages, such that, for example, binary number 1 equals 1 volt, binary number

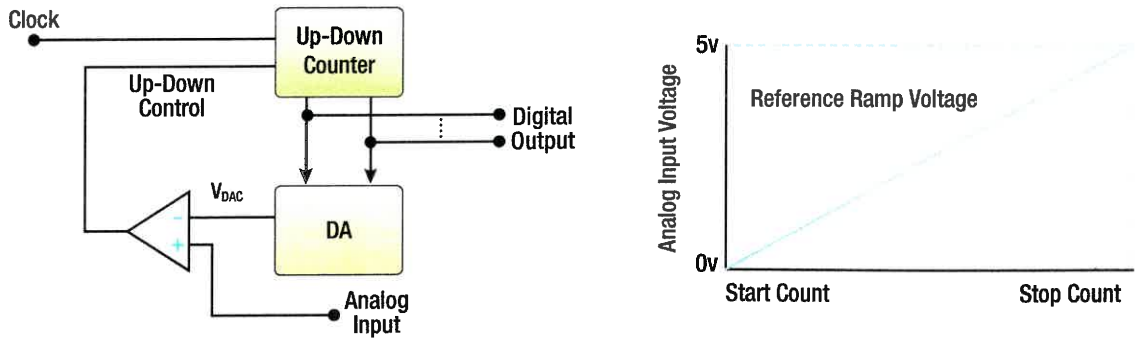


Figure 3-6. Integrating ADC Circuit (left) and Reference Ramp (right).

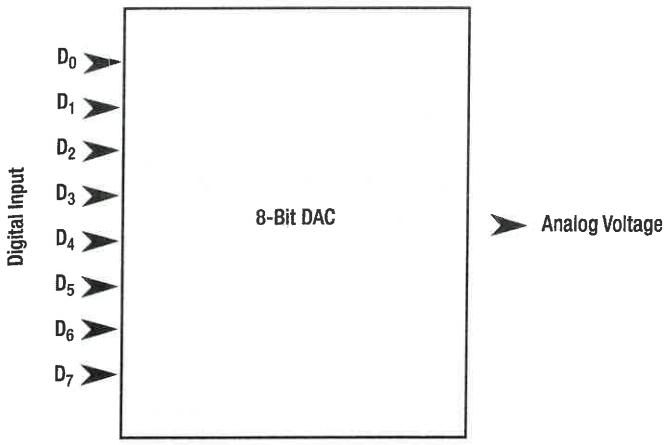
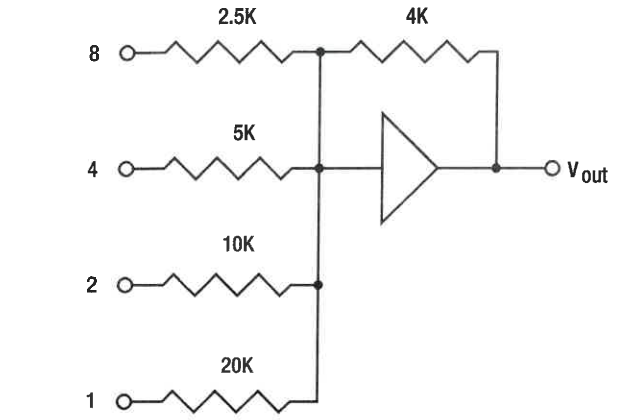


Figure 3-7. 8-Bit digital-to-analog converter symbol.

2 equals 2 volts, binary number 3 equals 3 volts, and so on. A typical DAC converts a sequence of binary digits (bits) into "impulses" that are then processed by a reconstruction filter to smooth out the step response into continuous curves. These impulses are created by updating the analog voltage output at uniform sampling intervals, controlled by a clock timing signal, which are then interpolated by a low-pass reconstruction filter to fill in the gaps between the impulses creating a continuously varied output. (***Figure 3-8***) Other DAC methods produce a pulse-modulated signal that can then be filtered in a similar way to produce a smoothly varying signal.

Figure 3-9 is a schematic diagram of a 4-bit resistor-ladder DAC with an op-amp. This DAC converts a binary input to a matching decimal number that corresponds to the output voltage. The numbers 1, 2, 4, and 8 refer to the relative weights assigned to each bit whereby input "1" is the Least Significant Bit (LSB) and input "8" is the Most Significant Bit (MSB). Thus if +5 volts (logic 1) is applied to input "1", the output will be 5 × (4 000 ohms/20 000 ohms) = 5 × 0.2 = 1 volt. If instead +5 volts is applied to input "2", the output will be 5 ×(4 000 ohms/10 000 ohms) = 5 × 0.4 = 2 volts. Similarly,



	BINARY NUMBER			
V out	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Figure 3-9. 4-Bit resistor-ladder DAC with voltage output table.

if either the "4" or "8" inputs are logic 1, then the output will be either 4 volts or 8 volts respectively. However, if +5 volts is applied to all 4 terminals simultaneously, the output will be 15 volts, representing the binary number input 1111. As a result, the output voltage can be one of 16 different voltages (including zero), in accordance with the input binary codes of 0000 through 1111 as shown on the corresponding table.

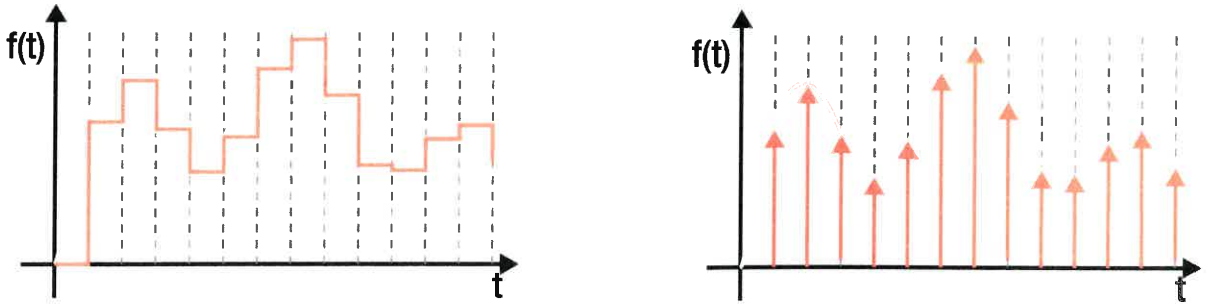


Figure 3-8. DAC output on left before reconstruction, and on right after reconstruction.

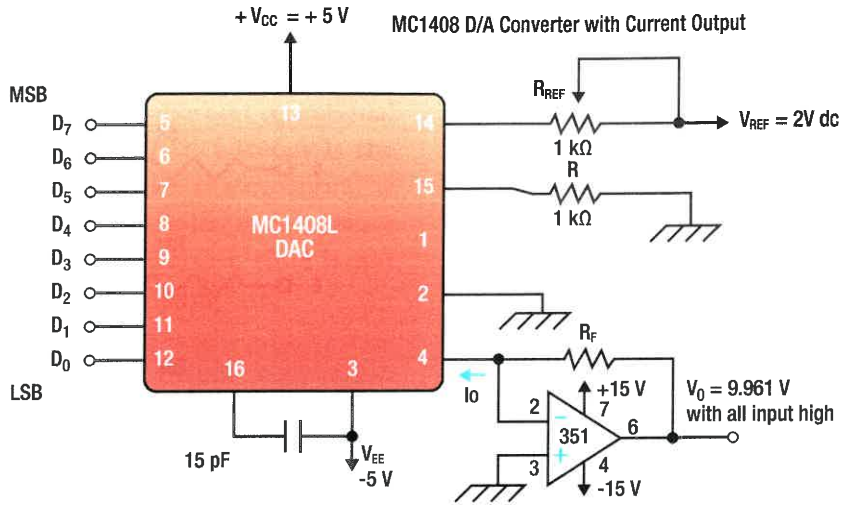


Figure 3-10. MC1408 8-bit DAC with Op-Amp.

The most commonly used 8-bit DAC is the MC1408, which has a current output that can be converted to a voltage type using a current-to-voltage converter op-amp. The MC1408 consists of a reference current amplifier, a resistor ladder, and 8 high-speed current switches. For many applications, only a reference resistor and reference voltage need to be added. (***Figure 3-10***)

LIMITATIONS OF CONVERSION

As previously discussed, analog signals are converted into digital signals so that the information is manipulated by instructions executed within a computer and then converted back to analog signals to drive analog display formats (such as hands on a clock) that are easily recognized by the crew. However, reconstructing a signal from digital-to-analog or from analog-to-digital can degrade the signal by introducing errors, also known as noise. Reconstruction noise, as well as sampling noise from quantization, not only combine in the final signal, but also compound over multiple stages of conversion resulting in a loss of quality, or fidelity, of the original signal. All though not apparent, the waveform shown at the bottom of ***Figure 3-11*** is a distorted version of the original waveform shown at the top of that figure.

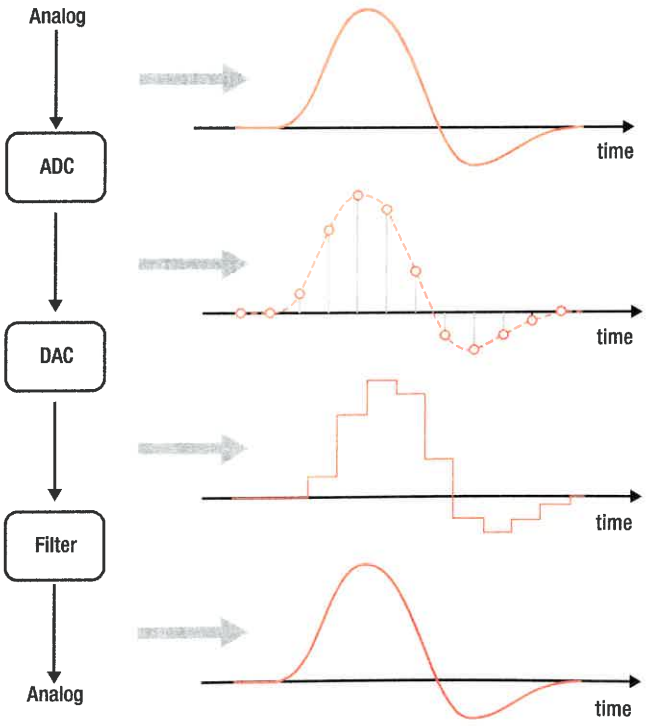


Figure 3-11. Conversion from analog to digital and back to analog.

An example of a system that converts analog signals to digital and back to analog is an in-flight entertainment (IFE) system.

When an announcement needs to be made, the microphone receives sound pressure from the crewmember's voice, which produces an analog audio signal. The ADC then converts the analog signal to a digital signal to be sent along a digital data bus to a computer whereby the signal is manipulated with other digital signals and sent along a digital data base to a DAC where it is converted back into an analog audio signal to drive the coil on the speaker to replicate the crewmember's voice. However, it is well known that the quality of the crewmember's voice on the microphone will always be of less fidelity as compared to hearing the crewmember speak in person. As such, it is important to recognize that signal degradation is a known limitation of multiple A/D and D/A conversions. (***Figure 3-12***)

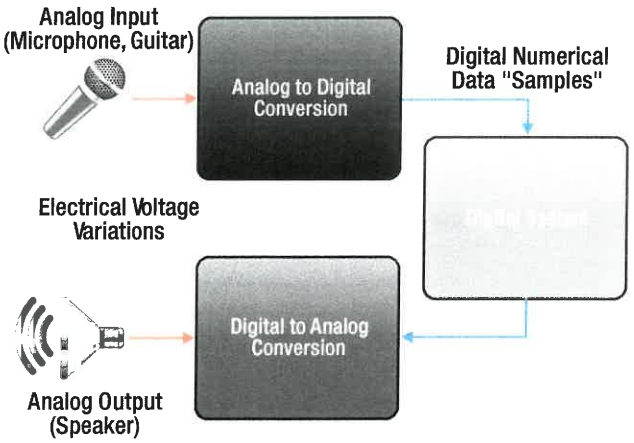


Figure 3-12. A/D conversion and then back to D/A conversion.

Question: 3-1
What is the difference between analog circuits and digital circuits?

Question: 3-2
Are DC (direct current) analog signals bipolar or unipolar?

Question: 3-3
Explain the device and process used to convert an analog signal to a digital signal.

Question: 3-4
How can quantization error be reduced in an Analog-to-Digital Converter (ADC)?

Question: 3-5
Compare and contrast the Direct Comparison Analog-to-Digital Converter (ADC) versus an Integrating ADC.

Question: 3-6
Explain the device and process used to convert a digital signal to an analog signal.

Question: 3-7
Explain the operation of a 4-bit resistor-ladder Digital-to-Analog Converter (DAC).

Question: 3-8
What are the limitations of using multiple Analog-to-Digital Converters and Digital-to-Analog Converters?

ANSWERS

Answer: 3-1
Analog circuits are different from digital circuits in that they do not have two set values, such as 0 volts representing "OFF" and 5 volts representing "ON". Instead, analog circuits will vary continuously in both time and value from high to low. Analog signals have the advantage in that they can represent any functional quantity, such as time, temperature, pressure, etc., by outputting an equivalent functional quantity of voltage or current.

Answer: 3-2
DC analog signals are unipolar in that they will have 0 volts as one of its limits with either a positive or a negative voltage defining its other analog signal voltage range limit. Whereas, AC (alternating current) analog signals can be bipolar in that they have both positive and negative limits as seen in an AC sine wave.

Answer: 3-3
An Analog-to-Digital Converter (ADC) is a device that converts a continuous input voltage to a digital data stream that represents the amplitude of the input analog signal. As such, the ADC performs conversions periodically by sampling and quantizing the input signal over a very short period of time. The result is a sequence of digital numbers that have been converted from continuous time and amplitude analog signals to discrete time and amplitude digital signals.

Answer: 3-4
Quantization error can be reduced by generating more bits per sample, with each bit occupying less of the overall voltage range. For example, a 14-bit ADC will sample 2^{14} or 16 384 voltage bands.

Answer: 3-5
The Direct Comparison ADC uses a resistor ladder to divide the reference voltage range into different voltage bins for sampling and quantization. The threshold detector in each op-amp then drives the encoding logic that detects the highest reference that is exceeded to derive the digital equivalent of the analog input voltage. The Integrating ADC is slower than the Direct Comparison ADC; however, its circuitry is less complex because it uses a digital counter to count the time it takes for a reference voltage to integrate a charge on a capacitor to the same value as the analog input voltage. The counter counts the clock pulses required until the op-amp comparator indicates that the ramp has reached the analog input voltage level. The number of clock pulses counted is the digital equivalent of the analog voltage input.

Answer: 3-6
A Digital-to-Analog Converter (DAC) is a device that reconstructs finite-precision time series data in to a continuously varying signal, which theoretically can have an infinite number of states. A typical DAC converts a sequence of binary digits (bits) into "impulses" that are then processed by a reconstruction filter to smooth out the step response into continuous curves. These impulses are created by updating the analog voltage output at uniform sampling intervals, controlled by a clock signal, which are then interpolated by a low-pass reconstruction filter to fill in the gaps between the impulses creating a continuously varied output.

Answer: 3-7
This DAC converts a binary input to a matching decimal number that corresponds to the output voltage. The inputs to ladder labeled 1, 2, 4 and 8 refer to the relative weights assigned to each bit whereby input "1" is the Least Significant Bit (LSB) and input "8" is the Most Significant Bit (MSB). As a result, the output voltage can be one of 16 different voltages (including zero), in accordance with the input binary numbers of 0000 through 1111.

Answer: 3-8
Reconstruction noise, as well as sampling noise from quantization, not only combine in the final signal, but also compound over multiple stages of conversion resulting in a loss of quality, or fidelity, of the original signal.

PART-66 SYLLABUS LEVELS

CERTIFICATION CATEGORY → B2

Sub-Module 04

DATA BUSES

Knowledge Requirements

5.4 - Data Buses

Operation of data buses in aircraft systems, including knowledge of ARINC and other specifications. Aircraft Network / Ethernet.	2

5.4 - DIGITAL DATA BUSES

An integrated avionics system consists of various subsystems and components that need to communicate with each other in order to share information. Up until the early 1970's, many avionic systems were largely analog implementations using syncho and potentiometer outputs and inputs with required point-to-point wiring between various sensors and their dedicated cockpit instruments. As such, there were many large and heavy wiring bundles with point-to-point wiring, in addition to reliability problems due to intermittent connector pin failures.

In order to reduce aircraft weight and increase reliability, it became necessary to decrease the amount of aircraft wiring and connectors. Therefore, avionics system designers began using Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs) with serial point-to-point digital data buses requiring only two twisted pairs of wires connecting single data transmitters (sources) and single data receivers (sinks). These data buses evolved into single-source with multiple-sink buses, such as ARINC 429, and multiple-source with multiple sinks buses, such as ARINC 629 and its military equivalent, MIL-STD-1553B.

Time-Division Multiplexing (TDM) enabled different forms of information to be transmitted through one communication system. A multiplexer was used to sample input data sequentially and then stagger the different data samples in time to form a composite digital pulse train. By knowing the clock time and address of the various signals, a de-multiplexer at the receiving end would decode and distribute the individual signals. The following sections will discuss several popular military and commercial aircraft digital data buses, beginning with MIL-STD-1553B.

MIL-STD-1553B

In 1975, the U.S. Air Force F-15 and F-16 tactical fighters were the first military aircraft to employ a digital data bus. The TDM concept had evolved from single data source and single data sink to multiple data sources and multiple data sinks residing on a single multiplex bus. This highly reliable serial data bus was originally developed by the U. S. Air Force Research Laboratory and McDonnell Douglas (now Boeing) as H009, and later in 1978, became a military standard, known as MIL-STD-1553B. It has a data transfer rate of 1 million bits per second (1 Mbps) and allows no more than 1 word fault per 10 million words.

MIL-STD-1553B is an asynchronous half-duplex bus, meaning that data can move in both directions, but only in one direction at a time. Full-duplex would mean that data can move in both directions at the same time. An example of half-duplex operation is a speakerphone that does not allow one to speak while another person is talking. However, a cell phone which is full duplex permits one to talk and listen simultaneously.

As shown in ***Figure 4-1***, the 1553B bus consists of a Bus Controller (BC) and up to 31 Remote Terminals (RT) which interface with the various subsystems. The Bus Controller (BC) initiates all data transfers by sending a command to a specified RT. Only the Remote Terminal receiving the command will respond. The command may include data or requests for data, and a status request from the RT. The RTs receive and decode the signals, reports errors and corrects them.

As the term implies, the Bus Monitor (BM) monitors the status of each transfer to determine that the data was successful transmitted and received error free. Typically,

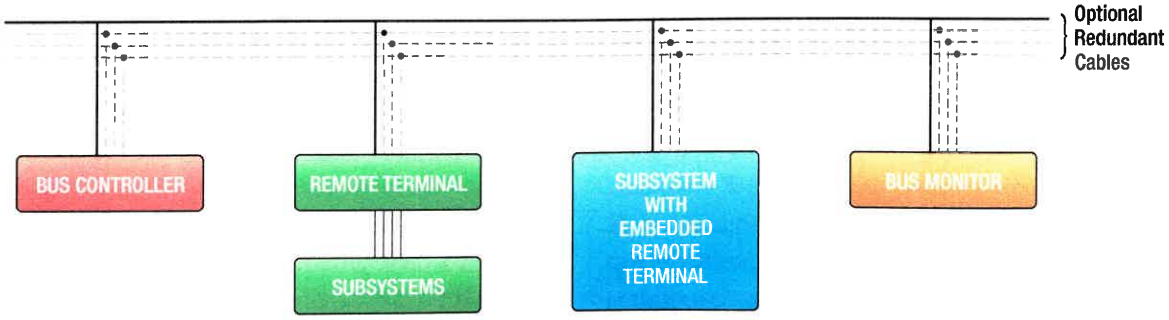


Figure 4-1. MIL-STD-1553B multiplex data bus topology.

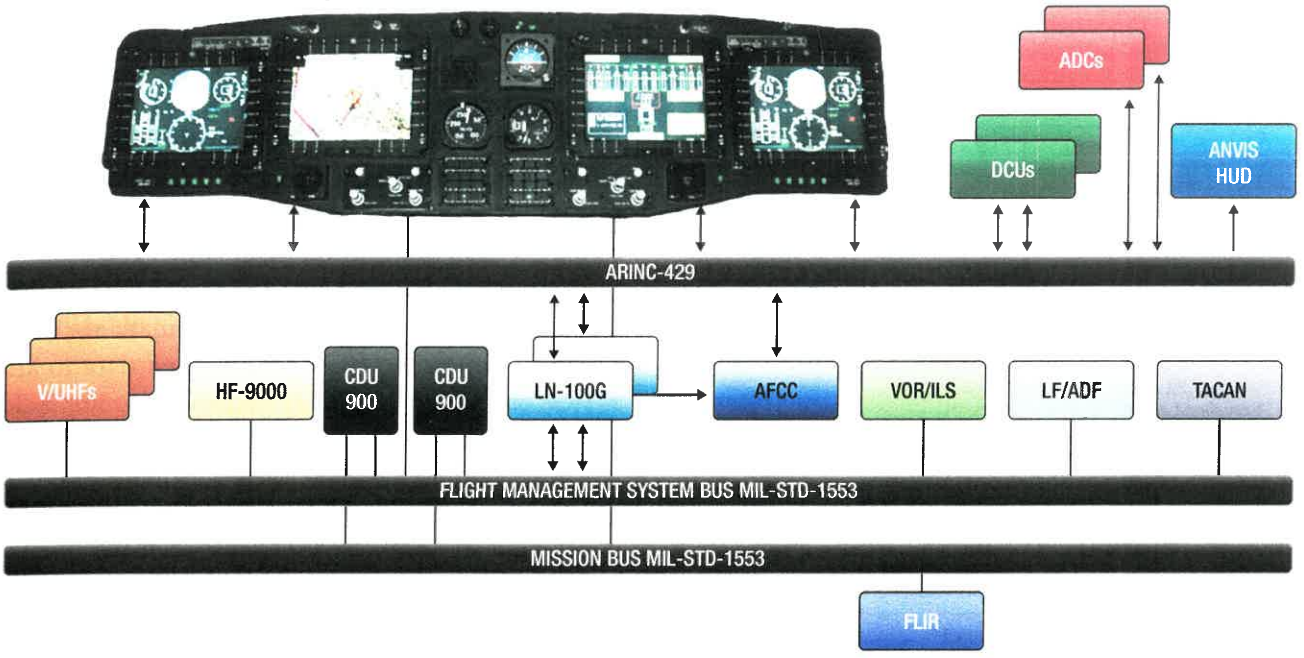


Figure 4-2. Sikorsky S-70 helicopter multi-level bus topology.

the Bus Monitor and the Bus Controller are physically located within the same "black box" or Line Replaceable Unit (LRU), often called a Mission Computer. The Mission Computer hosts the entire avionics software operating system, known as an Operational Flight Program (OFP).

Topology refers to the physical layout and connections of each device to the bus. ***Figure 4-1*** illustrates a single-level topology. Multiple level topologies are formed by interconnecting single-level buses so data from one bus can be transferred on to another bus. Multi-level buses are used to isolate flight-critical flight management functions from non-flight critical mission-related functions. (***Figure 4-2***)

Each level will have two or more separate redundant buses, so that a secondary bus can take over communications in the event that the primary bus fails. For example, if the BM receives an error message, the BC may attempt to resend its command signal over a secondary backup bus. Also, it is not uncommon to have a back-up BC/BM as well, although only one BC will have command-response authority over the buses at any one time. The bus cables are shielded twisted-wire pairs with the shields grounded at both ends. Every device must be coupled to the bus using an isolation transformer to avoid the risk of taking the down the bus if a device short-circuits. Isolation transformers can be either directly coupled (***Figure 4-3***) with no more than a 1 foot stub length, or transformer coupled (***Figure 4-4***) with a maximum stub length of 20 feet.

Information is transmitted between the BC and the RTs or from RT to RT using composite digital pulse trains consisting of 20-bit command words, data words, and status words using one of the six information transfer formats shown in ***Figure 4-5***.

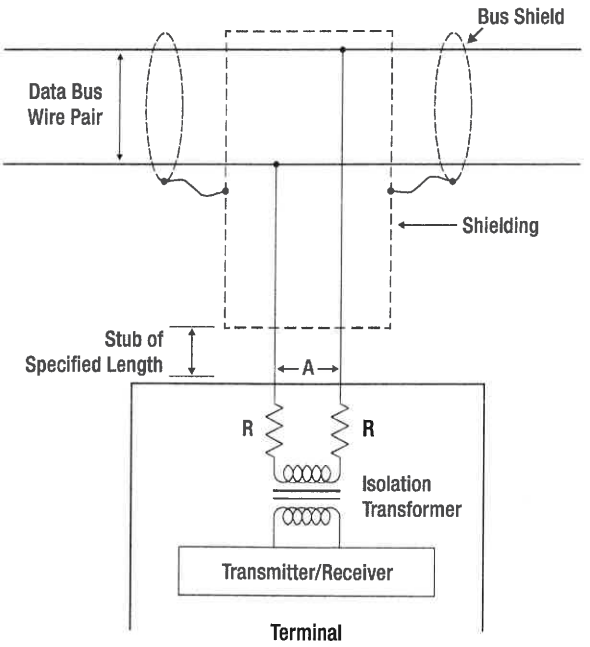


Figure 4-3. Data bus interface using direct coupling.

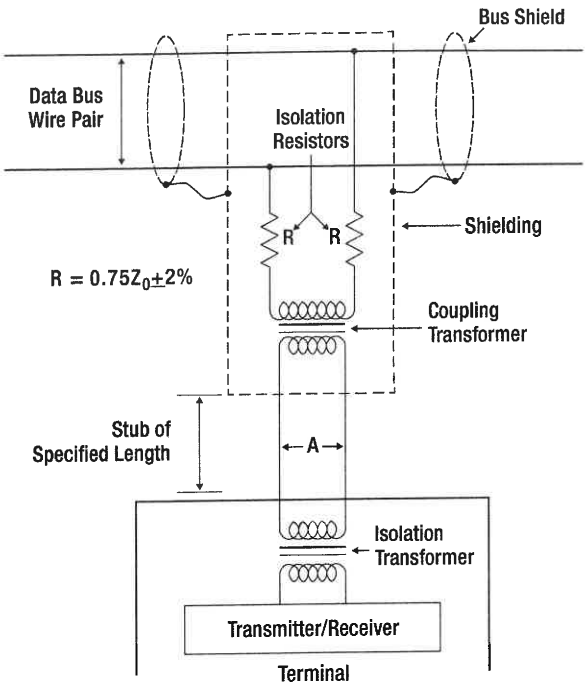


Figure 4-4. Data bus interface using transformer coupling.

The command word tells the RT to receive data, transmit data, or to switch modes. There can be up to 32 data words sent or received following a command. The RT responds with a status word for error checking. For the BC to command an RT to send data to another RT, the BC must first send a receive command followed by a transmit command, since RTs don't have the capability to initiate data transfers on their own.

Broadcast information transfer formats are used on occasions when the BC needs to send data to all the RTs at once. (***Figure 4-6***) A status word is not included in these broadcast commands because if all the RTs responded at once it would cause data collisions to occur on the bus.

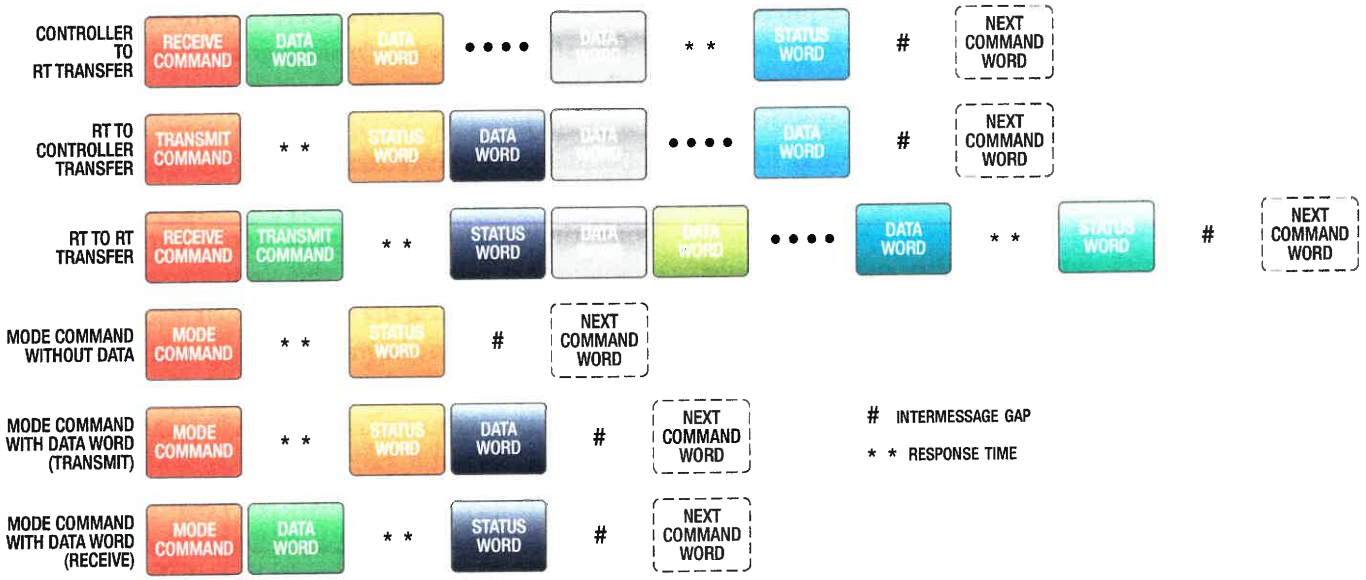


Figure 4-5. Information transfer formats.

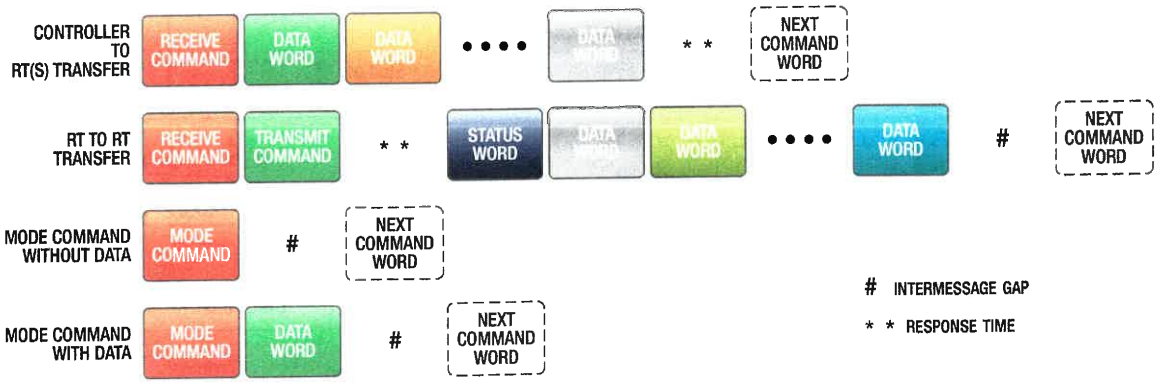


Figure 4-6. Broadcast information transfer formats.

ARINC 429

Aeronautical Radio Incorporated (ARINC) was formed in 1929 as a non-profit organization with airline and aircraft industry representation to develop standards for equipment form, fit and function compatibility and environmental operational specifications. ARINC developed the A429 digital data bus, used in the Boeing 757/767 and Airbus A300/A310, as a commercial aircraft standard. It is less complex and less costly than MIL-STD-1553B. However, it has its limitations.

A429 is not as robust as 1553B as it can only accept up to 20 receiver terminals, and its data rate is limited to 100 000 bits per second (100 Kbps). It has a self-clocking, self-synchronizing data bus protocol similar to 1553B, and it uses shielded twisted-pair wires for a physical connection. The major limitation of A429 is that it has a simplex architecture, meaning that digital data can travel only in one direction from the transmitter source to the receiver sink at any one time; data can't travel in the opposite direction on the same bus.

What this means is that if there are multiple sinks for one source and one of those sinks needs to transmit back to the source and/or the other sinks, it will need a separate twisted-pair wire to do so since data transfer is not bi-directional. (***Figure 4-7***)

A429 uses a return-to-zero modulation technique to form each bit meaning that logic state "1" is achieved by voltage moving from high (e.g., +10 volts) to null (zero volts) and logic state "0" is obtained by going from null to low (e.g., -10 volts). ***Figure 4-8*** illustrates how an ARINC 429 data word is formed. The first bit is the parity bit (used for error detection), followed by three sign and status matrix bits, 18 data bits, 2 bits for the source destination identifier and an 8 bit data word label.

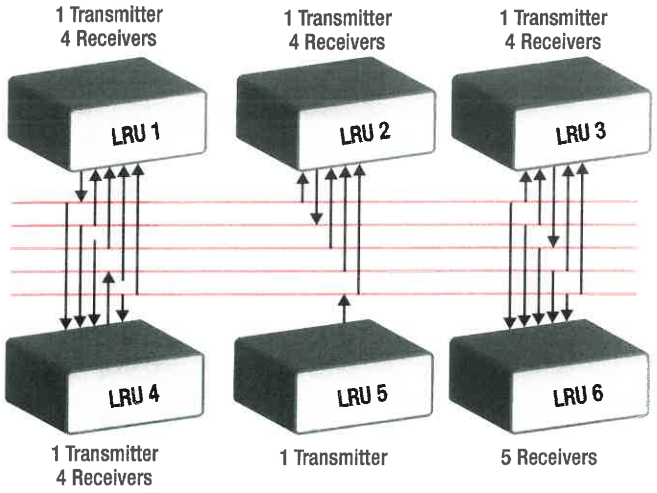


Figure 4-7. ARINC 429 has a simplex digital data bus topology.

A message consists of a start-of-transmission signal, up to 253 data words, and an end-of-transmission signal.

ARINC 629

The newer A629 data bus, used in the Boeing 777, has a data rate of 2 Mbps, which is 20 times faster than A429, and can handle 131 terminals instead of only 20.

As shown in ***Figure 4-9***, A629 has a multiple-source and multiple-sync bus topology that is very similar to MIL-STD-1553B, except that it does not have a Bus Controller/Monitor, and separate channels must be used to transmit and receive. A629 uses a time-based, collision-avoidance protocol that allocates an assigned time slot to each terminal in which it is allowed to transmit on to the data bus. Each terminal decides when an appropriate time slot is available for transmission. Terminals are connected to the bus via a Serial Interface Module to provide isolation so that a shorted terminal can't bring down the entire bus. A629 data words consist of 3 sync bits, 16 data bits, and 1 parity bit.

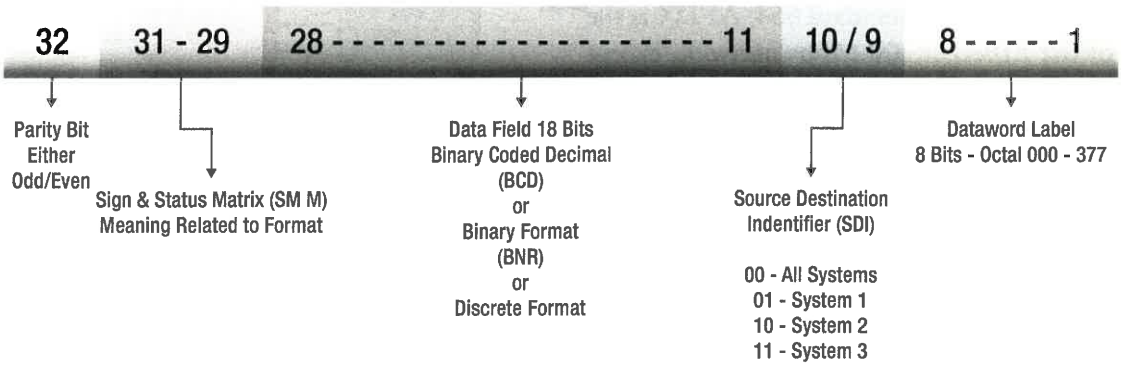


Figure 4-8. ARINC 429 32-bit data word format.

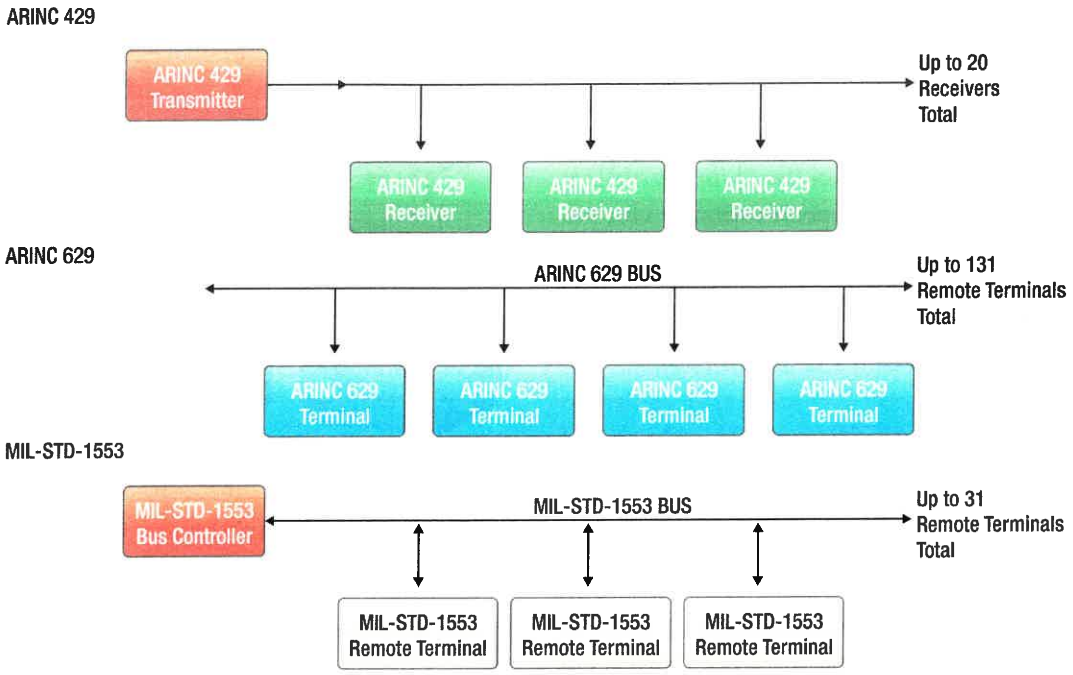


Figure 4-9. Comparison of A429, A629, and 1553B data bus topologies.

AIRCRAFT NETWORKS/ETHERNET

Ethernet is a commercial computer networking technology for local area and larger networks that was first introduced in 1980. In 1983, it became standardized by the Institute of Electrical and Electronic Engineers as IEEE 802.3. The original concept used coaxial cables as a shared medium. It has since evolved to using either twisted-pair wires (for low-speed data transfer) or fiber-optic cables (for higher speeds) in conjunction with the use of hubs or switches. The data transfer speed has also since increased from 2 Mbps to 100 Mbps. Each data frame contains of a source address and destination address, in addition to error checking so that damaged data can be detected and the data frame retransmitted if required.

ARINC 664 AFDX

The Avionics Full-Duplex Switched (AFDX) network, currently being used in the Airbus A380 and the Boeing 787, is specified as ARINC Standard 664. AFDX is the equivalent of the Ethernet 100 Mbps network, except that it has been adapted with deterministic timing and redundancy required for avionics applications. AFDX works more like a telephone exchange network than a typical aircraft digital data bus with data being switched from subscriber to subscriber, except that the subscribers are Line Replaceable Units (LRU).

As shown in ***Figure 4-10***, the AFDX network topology consists of switches for traffic policing and LRU terminals (end systems) for traffic shaping and integrity checking. The switches and the terminals communicate with each other simultaneously (full-duplex) to prevent data collisions. Data transfer is accomplished via 'virtual links", which are unidirectional connections from one source terminal to one or more destination terminals. Virtual links are determined by fixed commutation tables that are resident in each switch. Configuration tables within each LRU terminal dictate the formatting of the data that is transmitted. AFDX data words will contain destination and source addresses and the frame size can be anywhere from 64 to 1518 bytes.

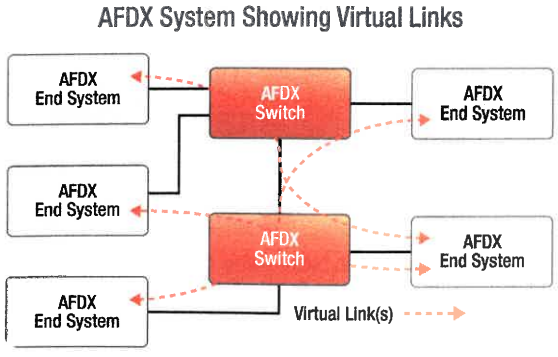


Figure 4-10. AFDX network topology.

IEEE 1394 FIREWIRE

Another commercial network that is making its way onboard aircraft is IEEE 1394, also known as Firewire. It was originally developed by the Institute of Electrical and Electronic Engineers (IEEE) for the consumer electronics industry as a serial point-to-point interface. It has since become popular for aircraft in-flight entertainment systems for streaming high-speed video signals due to its high data rate of up to 800 Mbps. The Firewire serial bus is also used in the Lockheed Martin F-35 Joint Strike Fighter Vehicle Management System for flight control, engine control and utility systems control, due to its large bandwidth and fault-tolerant topology where no single point failure can bring down the entire bus.

Question: 4-1
What are the advantages of using digital data buses over point-to-point wiring?

Question: 4-2
What is Time-Division Multiplexing (TDM) and how does it work?

Question: 4-3
Is MIL-STD-1553B a full-duplex or half-duplex bus and what is the difference?

Question: 4-4
Describe how the MIL-STD-1553B command-response protocol operates.

Question: 4-5
Why is the reason for having multiple-level topology buses?

Question: 4-6
What is the major limitation of ARINC 429?

Question: 4-7
What are the major differences between ARINC 629 and other digital data buses?

Question: 4-8
Explain the operation of the Avionics Full-Duplex Switched (AFDX) network.

ANSWERS

Answer: 4-1
Up until the early 1970's, there were many large and heavy wiring bundles with point-to-point wiring that presented reliability problems due to intermittent connector pin failures. In order to reduce aircraft weight and increase reliability, it became necessary to decrease the amount of aircraft wiring and connectors with serial point-to-point digital data buses requiring only two twisted pairs of wires connecting data transmitters (sources) and data receivers (sinks).

Answer: 4-2
TDM enables different forms of information to be transmitted through one communication system. A multiplexer is used to sample input data sequentially and then stagger the different data samples in time to form a composite digital pulse train. By knowing the clock time and address of the various signals, a de-multiplexer at the receiving end decodes and distributes the individual signals.

Answer: 4-3
MIL-STD-1553B is an asynchronous half-duplex bus, meaning that data can move in both directions, but only in one direction at a time. Full-duplex would mean that data can move in both directions at the same time.

Answer: 4-4
The Bus Controller (BC) initiates all data transfers by sending a command to a specified RT. Only the Remote Terminal (RT) receiving the command will respond. The command may include data or requests for data, and a status request from the RT. The RTs receive and decode the signals, reports errors and corrects them.

Answer: 4-5
Multiple level topologies are formed by interconnecting single-level buses so data from one bus can be transferred on to another bus. Multi-level buses are used to isolate flight-critical flight management functions from non-flight critical mission-related functions. Each level will have two or more separate redundant buses, so that a secondary bus can take over communications in the event the primary bus fails.

Answer: 4-6
The major limitation of A429 is that it has a simplex architecture, meaning that digital data can travel only in one direction from the transmitter source to the receiver sink at any one time; data can't travel in the opposite direction on the same bus. What this means is that if there are multiple sinks for one source and one of those sinks needs to transmit back to the source and/or the other sinks, it will need a separate twisted-pair wire to do so since data transfer is not bi-directional.

Answer: 4-7
The A629 data bus has a data rate of 2 Mbps, which is 20 times faster than A429, and can handle 131 terminals instead of only 20. A629 is has a multiple-source and multiple-sync bus topology that is very similar to MIL-STD-1553B, except that it does not have a Bus Controller/Monitor, and separate channels must be used to transmit and receive. A629 uses a time-based, collision-avoidance protocol that allocates an assigned time slot to each terminal in which it is allowed to transmit on to the data bus. Each terminal decides when an appropriate time slot is available for transmission.

Answer: 4-8
The AFDX network topology consists of switches for traffic policing and LRU (Line Replaceable Units) terminals for traffic shaping and integrity checking. The switches and the terminals communicate with each other simultaneously (full-duplex) to prevent data collisions. Data transfer is accomplished via 'virtual links", which are unidirectional connections from one source terminal to one or more destination terminals. Virtual links are determined by fixed commutation tables that are resident in each switch. Configuration tables within each LRU terminal dictate the formatting of the data that is transmitted. AFDX data words will contain destination and source addresses and the frame size can be anywhere from 64 to 1518 bytes.

DIGITAL TECHNIQUES ELECTRONIC INSTRUMENT SYSTEMS

LOGIC CIRCUITS

SUB-MODULE 05

PART-66 SYLLABUS LEVELS

CERTIFICATION CATEGORY → B2

Sub-Module 05

LOGIC CIRCUITS

Knowledge Requirements

5.5 - Logic Circuits

(a)	Identification of common logic gate symbols, tables and equivalent circuits; Applications used for aircraft systems, schematic diagrams.	2
(b)	Interpretation of logic diagrams.	2

5.5 - LOGIC GATES

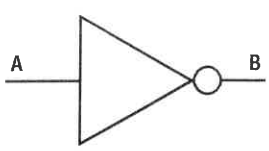
A gate is a special type of circuit designed to accept and generate voltage signals corresponding to binary 1's and 0's. Transistors are used in digital electronics to construct circuits that act as digital logic gates. The purpose and task of the device is achieved by manipulating electric signals through the logic gates. Thousands, and even millions, of tiny transistors can be placed on a chip to create the digital logic landscape through which a component's signals are processed.

As explained in *Sub-Module 02*, digital logic is based on the binary number system. There are two conditions than may exist, 1 or 0. In a digital circuit, these are equivalent to voltage or no voltage. Within the binary system, these two conditions are called Logic 1 and Logic 0. Using just these two conditions, gates can be constructed to manipulate information. There are a handful of common logic gates that are used. By combining any number of these tiny solid-state gates, significant memorization, manipulation, and calculation of information can be performed. A brief discussion of logic gates, their symbols, and truth tables follow.

NOT GATE

The NOT gate, also known as an 'inverter", is the simplest of all gates. If the input to the gate is Logic 1, then the output is NOT Logic 1. This means that it is Logic 0, since there are only two conditions in the binary world. In an electronic circuit, a NOT gate would invert the input signal. In other words, if there was voltage at the input to the gate, there would be no output voltage. The gate can be constructed with transistors and resistors to yield this electrical logic every time. (The gate or circuit would also have to invert an input of Logic 0 into an output of Logic 1.)

To understand logic gates, truth tables are often used. A truth table gives all of the possibilities in binary terms for each gate containing a characteristic logic function. For example, a truth table for a NOT gate is illustrated in ***Figure 5-1.*** Any input (A) is NOT present at the output (B). This is simple, but it defines this logic situation. A tiny NOT gate circuit can be built using transistors that produce these results. In other words, a circuit can be built such that if voltage arrives at the gate, no voltage is output or vice-versa.



The Not Gate

A	B
1	0
0	1

Figure 5-1. A NOT logic gate symbol and a NOT gate truth table.

When using transistors to build logic gates, the primary concern is to operate them within the circuits so the transistors are either OFF (not conducting) or fully ON (saturated). In this manner, reliable logic functions can be performed. The variable voltage and current situations present during the active mode of the transistor are of less importance.

Figure 5-2 illustrates an electronic circuit schematic diagram that performs the logic NOT gate function. Any input, either a no voltage or voltage condition, yields the opposite output. This gate is built with bipolar junction transistors, resistors, and a few diodes. Other designs exist that may have different components. When examining and discussing digital electronic circuits, the electronic circuit design of a gate is usually not presented. The symbol for the logic gate is most often used. The technician can then concentrate on the configuration of the logic gates in relation to each other.

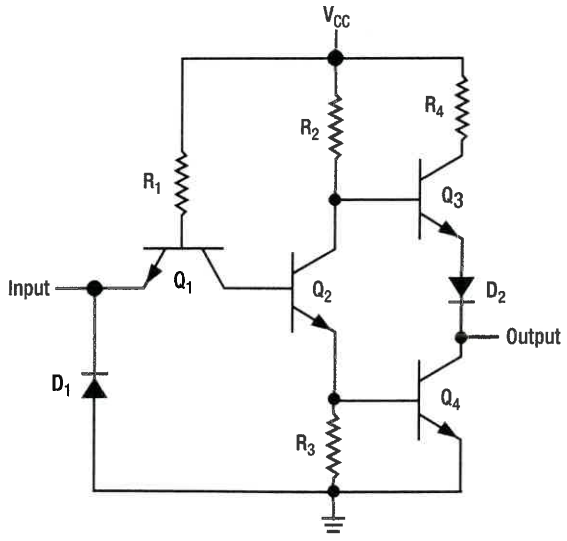
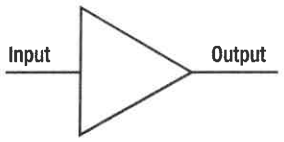


Figure 5-2. An electronic circuit that reliably performs the NOT logic function.

BUFFER GATE

Another logic gate with only one input and one output is the buffer. It is a gate with the same output as the input. While this may seem redundant or useless, an amplifier may be considered a buffer in a digital circuit because if there is voltage present at the input, there is an output voltage. If there is no voltage at the input, there is no output voltage. When used as an Operational Amplifier, the buffer can change the values of a signal. This is often done to stabilize a weak or varying signal. All gates are amplifiers subject to output fluctuations. The buffer steadies the output of the upstream device while maintaining its basic characteristic. Another application of a buffer, using two NOT gates, in series, is to use it to isolate a portion of a circuit. (***Figure 5-3***)



The BUFFER Gate

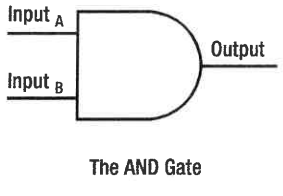
Input	Output
0	0
1	1

Figure 5-3. A buffer or amplifier symbol and the truth table of the buffer, which is actually two consecutive NOT gates.

An Operational Amplifier (OpAmp) is a high-gain differential voltage amplifier. The output can be hundreds or thousands times greater than the voltage of its input. The output is also linear with the difference between the input potential. They are widely used in a wide variety of electronic circuits including signal processing circuits, control circuits and instrumentation.

AND GATE

Most common logic gates have two inputs. Three or more inputs are possible on some gates. When considering the characteristics of any logic gate, an output of Logic 1 is sought and a condition for the inputs is stated or examined. For example, ***Figure 5-4*** illustrates an AND gate with a schematic representation of two switches in series.



The AND Gate

Input		Output
A	B	
0	0	0
0	1	0
1	0	0
1	1	1

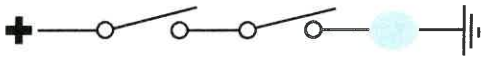


Figure 5-4. An AND gate symbol and its truth table with schematic diagram.

For an AND gate to have a Logic 1 output, both inputs have to be Logic 1. In an actual electronic circuit, this means that for a voltage to be present at the output, the AND gate circuit has to receive voltage at both of its inputs. As pointed out, there are different arrangements of electronic components that yield this result. Whichever is used is summarized and presented as the AND gate symbol. The truth table in ***Figure 5-4*** illustrates that there is only one way to have an output of Logic 1 or voltage when using an AND gate.

An example of AND logic could possibly be engage logic, found in an autopilot. In this case, the autopilot would not be allowed to be engaged unless certain conditions are first met. Such conditions could be: Vertical gyro is valid AND directional gyro is valid AND all autopilot control knobs are in depths AND servo circuits are operational. Only when these conditions are met will the autopilot be engaged. ***Figure 5-5*** Shows the logic of this system found in the aircraft wiring diagrams.

OR GATE

Another useful and common logic gate is the OR gate. In an OR gate, to have an output of Logic 1 (voltage present), one of the inputs must be Logic 1. As seen in ***Figure 5-6***, only one of the inputs needs to be Logic 1 for there to be an output of Logic 1. When both inputs are Logic 1, the OR gate has a Logic 1 output because it still meets the condition of one of the inputs being Logic 1.

Figure 5-7 is a simplified circuit that illustrates the OR logic. The example used is a "DOOR UNSAFE" annunciator. Let's say in this case that the plane has one cabin door and a baggage door. In order for the annunciator light on the master warning panel to extinguish, both doors must be closed and locked. If any one of the doors is not secured properly, the baggage door OR the cabin door, then the "DOOR UNSAFE" annunciator will illuminate.

In this case, two switches are in parallel with each other. If neither on of the two switches is closed, the light bulb will light up. The lamp will be off only when both switches are open.

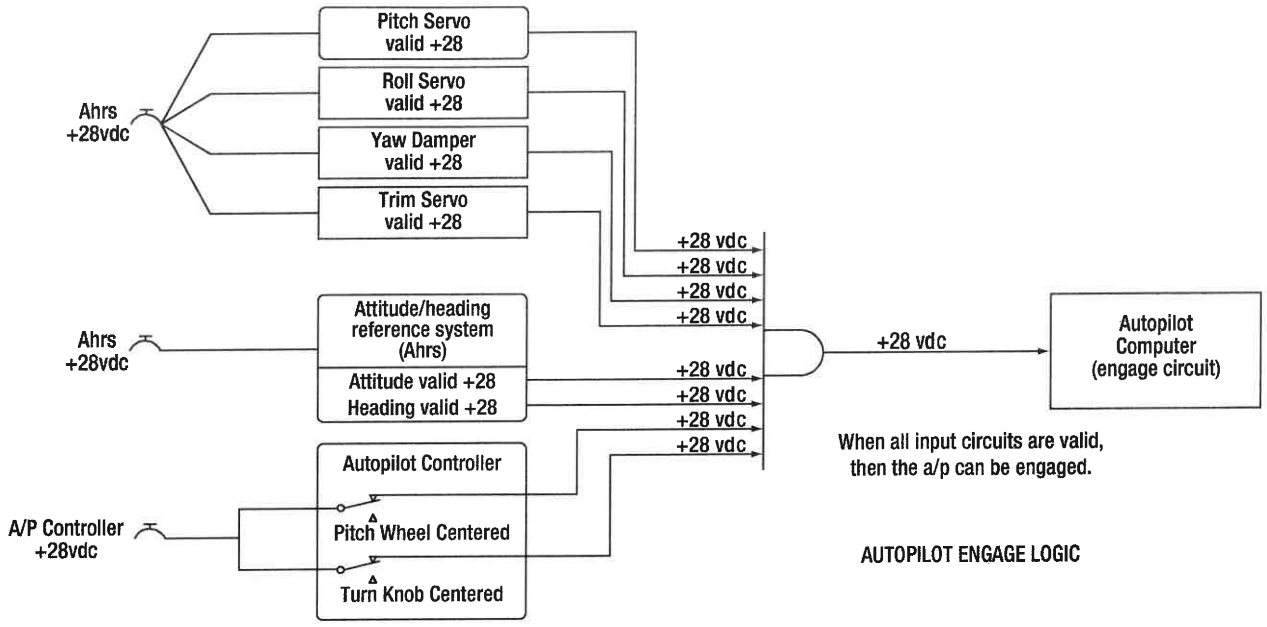
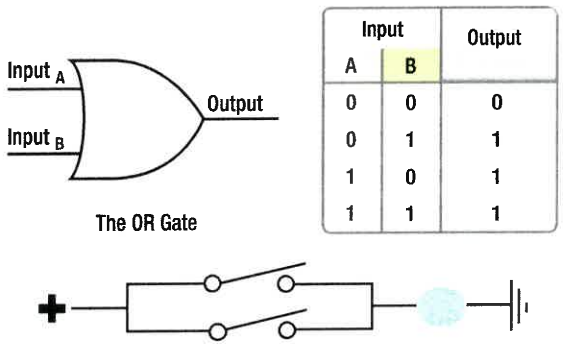


Figure 5-5. AND logic of system found in the aircraft wiring diagrams.



Input		Output
A	B	
0	0	0
0	1	1
1	0	1
1	1	1

Figure 5-6. An OR gate symbol and its truth table with schematic diagram.

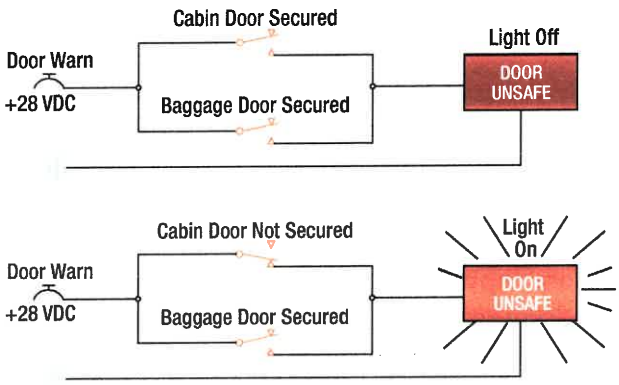
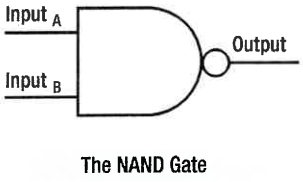


Figure 5-7. Simplified circuit that illustrates OR logic.

NAND GATE

The AND, OR, and NOT gates are the basic logic gates. A few other logic gates are also useful. They can be derived from combining the AND, OR, and NOT gates. The NAND gate is a combination of an AND gate and a NOT gate. This means that AND gate conditions must be met and then inverted. So, the NAND gate is an AND gate followed by a NOT gate. The truth table for a NAND gate is shown in ***Figure 5-8*** along with its symbol. If a Logic 1 output is to exist from a NAND gate, inputs A and B must not both be Logic 1. Or, if a NAND gate has both inputs Logic 1, the output is Logic 0. Stated in electronic terms, if there is to be an output voltage, then the inputs cannot both have voltage or, if both inputs have voltage, there is no output voltage.



Input		Output
A	B	
0	0	1
0	1	1
1	0	1
1	1	0

Figure 5.8. A NAND gate symbol and its truth table illustrating that the NAND gate is an inverted AND gate.

NOTE: The values in the output column of the NAND gate table are exactly the opposite of the output values in the AND gate truth table.

NOR GATE

A NOR gate is similarly arranged except that it is an inverted OR gate. If there is to be a Logic 1 output, or

output voltage, then neither input can be Logic 1 or have input voltage. This is the same as satisfying the OR gate conditions and then putting the output through a NOT gate. The NOR gate truth table in ***Figure 5-9*** shows that the NOR gate output values are exactly the opposite of the OR gate output values.

EXCLUSIVE OR GATE

Another common logic gate is the EXCLUSIVE OR (XOR) gate. It is the same as an OR gate except for the condition where both inputs are Logic 1. In an OR gate, there would be a Logic 1 when both inputs are Logic 1. This is not allowed in an EXCLUSIVE OR gate. When either of the inputs is Logic 1, the output is Logic 1. However, with an EXCLUSIVE OR gate, if both inputs are Logic 1, the Logic 1 output is excluded and results in Logic 0. (***Figure 5-10***)

EXCLUSIVE NOR GATE

The EXCLUSIVE NOR (X-NOR) gate is nothing more than an XOR gate with an inverted output. It produces a 1 output when all inputs are 1s and also when all inputs are 0s. The standard symbol and truth table is shown in ***Figure 5-11***. "T" is the time interval of the pulse.

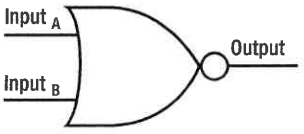
NEGATIVE LOGIC GATES

There are also negative input logic gates. The negative OR and the negative AND gates are gates wherein the inputs are inverted rather than inverting the output. Negative logic gates are used when the inputs need to be buffered or isolated. This creates a unique set of outputs as seen in the truth tables in ***Figure 5-12***.

The negative OR gate is not the same as the NOR gate as is sometimes misunderstood. Neither is the negative AND gate the same as the NAND gate. However, as the truth tables reveal, the output of a negative AND gate is the same as a NOR gate, and the output of a negative OR gate is the same as a NAND gate.

INTERPRETATION OF LOGIC DIAGRAMS

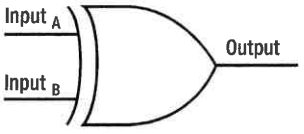
Electronic circuits use transistors to construct logic gates that produce outputs related to the inputs shown in the truth tables for each kind of gate. The gates are then assembled with other components to manipulate data in digital circuits. The electronic digital signals used are voltage or no-voltage representations of Logic 1 or Logic 0 conditions. By using a series of voltage and/or no-voltage outputs, a logic circuit manipulates, computes, and stores data.



The NOR Gate

Input A	Input B	Output
0	0	1
0	1	0
1	0	0
1	1	0

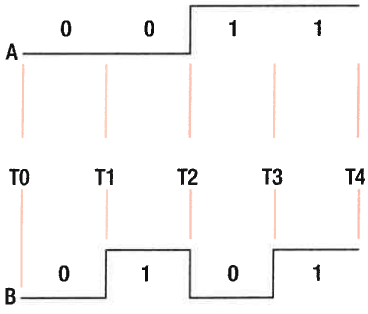
Figure 5-9. A NOR gate symbol and its truth table illustrating that the NOR gate is an inverted OR gate.



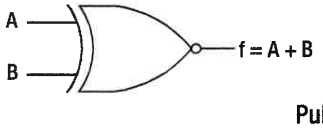
The Exclusive OR Gate

Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	0

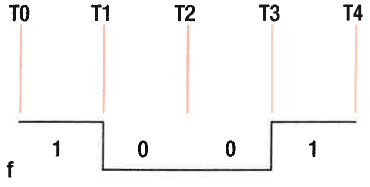
Figure 5-10. An EXCLUSIVE OR gate symbol and its truth table, which is similar to an OR gate but excludes output when both inputs are the same.



Pulse Train Timing Diagram



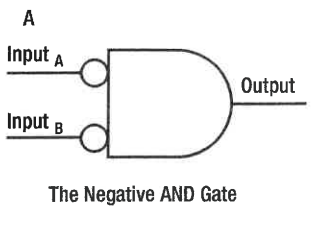
X-NOR gate input/output



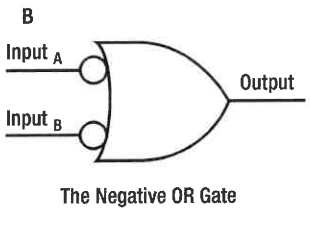
Pulse	A	B	f
T_1	0	0	1
T_2	0	1	0
T_3	1	0	0
T_4	1	1	1

Truth Table

Figure 5-11. An EXCLUSIVE NOR gate symbol and its truth table, which is an EXCLUSIVE OR gate with the output inverted.



Input		Output
A	B	
0	0	1
0	1	0
1	0	0
1	1	0



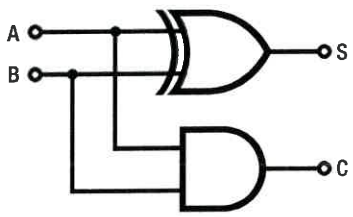
Input		Output
A	B	
0	0	1
0	1	1
1	0	1
1	1	0

Figure 5-12. The NEGATIVE AND gate symbol and its truth table (A) and the NEGATIVE OR gate symbol and truth table (B). The inputs are inverted in the NEGATIVE gates.

ADDER LOGIC CIRCUITS

An example of this is the half-adder logic circuit, shown in ***Figure 5-13***, consisting of an EXCLUSIVE OR (XOR) gate and an AND gate. As seen from the truth table, voltage applied to either input A or B will cause the sum (S) to be 1. Voltage applied to both A and B will cause S to be 0 and the carry (C) to be 1 forming the binary number 10, which is the decimal number 2. Half-adders can only add two digits. A full-adder becomes necessary when a carry input (Cin) must be added to the two binary digits to obtain a decimal sum of 3. In this case, a full-adder logic circuit can be constructed from two half-adders and an OR gate, shown in ***Figure 5-14***.

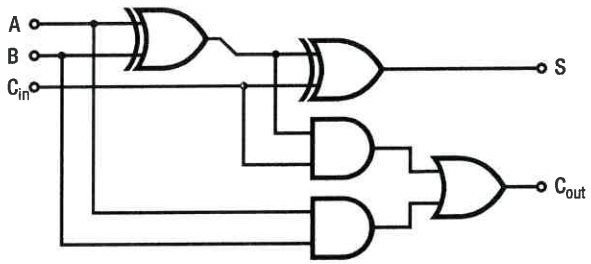
It is worth noting again that an advantage of digital components and circuits is that voltage and current flow does not need to be exact. Positive voltage between 2.6 and 5.0 volts at the input of a gate is considered an input signal of Logic 1. Any voltage less than 2.5 volts at the gate input is considered no voltage or an input of Logic 0.



HALF-ADDER TRUTH TABLE

A	B	C	S
0	0	0	0
1	0	0	1
0	1	0	1
1	1	1	0

Figure 5-13. Half-adder logic circuit used for adding two numbers.



FULL-ADDER TRUTH TABLE

A	B	Cin	Cout	Sout
0	0	0	0	0
0	1	0	0	1
1	0	0	0	1
1	1	0	1	1
0	0	1	0	1
0	1	1	1	0
1	0	1	1	0
1	1	1	1	1

Figure 5-14. Full-adder logic circuit for adding three numbers.

TTL AND CMOS

There are several different kinds of logic circuits, the most popular being TTL (transistor-transistor logic) and CMOS (complementary metal oxide semiconductor). TTL logic circuit elements are primarily bipolar semiconductor components connected together to produce a consistent output. This output may be combined with the output of other TTL logic elements and logic circuits to perform a task. TTL circuits operate with +5-volts power source. It uses positive logic, meaning Logic 1 occurs with +5 volts and Logic 0 is ground or 0 volts. There are different types of TTL circuits that have different power requirements.

CMOS logic circuits are constructed with metal oxide semiconductor transistors rather than the bipolar junction transistors used in TTL. CMOS logic circuits use less power because of the construction of the logic gates and, therefore, the digital circuits that are comprised of CMOS components use fewer elements. CMOS transistor output is triggered by lower voltage and does not rely on current flow through the base-emitter junction.

The same digital logic results as TTL circuits is accomplished, but CMOS logic circuits are less susceptible to electrical interference and operate with a wider range of voltages (Logic 1 between +3 and +18 volts). CMOS technology is predominant in modern integrated circuits used in aircraft systems.

AIRCRAFT LOGIC CIRCUIT APPLICATIONS

One example of logic circuits applied to aircraft applications would be illuminating display segments of numbers on a radio control head. The circuit shown in ***Figure 5-15*** uses a NOT gate and three OR gates. Feeding patterns of binary numbers into the four inputs on the left will turn the segment "ON" and "OFF". For example, feed in the decimal number 7 as four binary inputs of "0111" and the gates will trigger as shown, switching "ON" the lower right display segment.

Another aircraft logic circuit application is the Landing Gear Warning Indicator. It consists of a 3-input NOR gate and a 3-Input AND gate, as shown in ***Figure 5-16***. As can be seen from the truth tables, when all 3 landing gear are extended and locked they each activate a limit switch which provides a voltage (1) to the 3 inputs of both gates thereby turning "OFF" (0) the red LED (light-emitting diode) and turning "ON" (1) the green LED. The opposite occurs when all three landing gear are retracted turning "ON" (1) the red LED and turning "OFF" (0) the green LED indicator.

The next Sub-Module will discuss computer technology whereby multiple gates are coupled together in integrated circuits and applied to the task of binary number storage in memory circuits and manipulation in computing circuits with each gate's output representing one binary digit (bit) of a multi-bit binary number called "machine language".

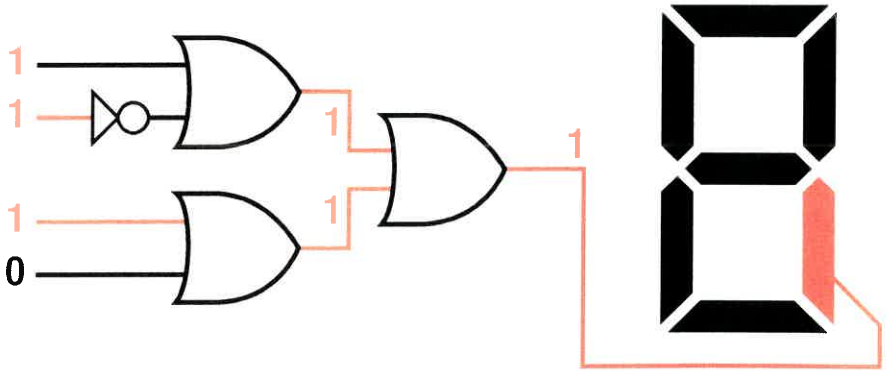
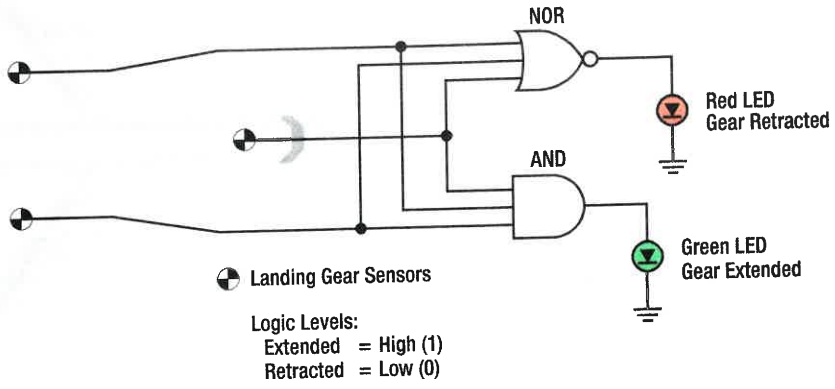


Figure 5-15. Logic circuit used on a radio control head.

Aircraft Logic Circuit
Landing Gear Warning Circuit



3-INPUT NOR GATE TRUTH TABLE

INPUT	INPUT	INPUT	OUTPUT
0	0	0	1
1	0	0	0
0	1	0	0
0	0	1	0
1	1	0	0
0	1	1	0
1	0	1	0
1	1	1	0

3-INPUT AND GATE TRUTH TABLE

INPUT	INPUT	INPUT	OUTPUT
0	0	0	0
1	0	0	0
0	1	0	0
0	0	1	0
1	1	0	0
0	1	1	0
1	0	1	0
1	1	1	1

Figure 5-16. Typical aircraft logic circuit for landing gear warning.

Question: 5-1
What is the difference between an inverter and a buffer?

Question: 5-2
Explain the logic function of the AND gate.

Question: 5-3
Explain the logic function of the OR gate.

Question: 5-4
Explain the logic function of the NAND gate.

Question: 5-5
Explain the logic function of the NOR gate.

Question: 5-6
What is the difference between an OR gate and an EXCLUSIVE OR gate?

Question: 5-7
What is the difference between the Negative OR and Negative AND gates and the NOR and NAND gates?

Question: 5-8
Explain the operation of a Half-Adder Logic Circuit.

ANSWERS

Answer: 5-1
An inverter, also known as a NOT gate, inverts the input signal. In other words, if there was voltage at the input to the gate, there would be no output voltage. A buffer is a gate with the same output as the input used to isolate or amplify a signal.

Answer: 5-2
For an AND gate to have a Logic 1 output, all inputs have to be Logic 1. In an actual electronic circuit, this means that for a voltage to be present at the output, the AND gate circuit has to receive voltage at all of its inputs.

Answer: 5-3
In an OR gate, only one of the inputs needs to be Logic 1 for there to be an output of Logic 1. When both inputs are Logic 1, the OR gate has a Logic 1 output because it still meets the condition of one of the inputs being Logic 1.

Answer: 5-4
The NAND gate is a combination of an AND gate and a NOT gate. This means that AND gate conditions must be met and then inverted. If a Logic 1 output is to exist from a NAND gate, inputs A and B must not both be Logic 1. Or, if a NAND gate has both inputs Logic 1, the output is Logic 0.

Answer: 5-5
A NOR gate is an inverted OR gate. If there is to be a Logic 1 output, or output voltage, then neither input can be Logic 1 or have input voltage. This is the same as satisfying the OR gate conditions and then putting the output through a NOT gate.

Answer: 5-6
An EXCLUSIVE OR (XOR) gate is the same as an OR gate, except for the condition where both inputs are Logic 1. In an OR gate, there would be a Logic 1 when both inputs are Logic 1. With an EXCLUSIVE OR gate, if both inputs are Logic 1, the Logic 1 output is excluded and results in Logic 0.

Answer: 5-7
The output of a Negative AND gate is the same as a NOR gate, and the output of a Negative OR gate is the same as a NAND gate. However, the inputs are inverted in the Negative OR and Negative AND gates.

Answer: 5-8
A Half-Adder Logic Circuit consists of an Exclusive OR (XOR) gate and an AND gate with their inputs connected in parallel. Voltage applied to either input will cause the sum to be 1. Voltage applied to both inputs will cause sum to be 0 and the carry to be 1 forming the binary number 10, which is the decimal number 2. Note: Half-adders can only add two digits. A full-adder becomes necessary when a carry input must be added to the two binary digits to obtain a decimal sum of 3.

PART-66 SYLLABUS LEVELS

CERTIFICATION CATEGORY → B2

Sub-Module 06

BASIC COMPUTER STRUCTURE

Knowledge Requirements

5.6 - Basic Computer Structure

(a)	Computer terminology (including bit, byte, software, hardware, CPU, IC, and various memory devices such as RAM, ROM, PROM); Computer technology (as applied in aircraft systems).	-
(b)	Computer related terminology; Operation, layout and interface of the major components in a micro computer including their associated bus systems; Information contained in single and multiaddress instruction words; Memory associated terms; Operation of typical memory devices; Operation, advantages and disadvantages of the various data storage systems.	2

5.6 - BASIC COMPUTER STRUCTURE

A computer accepts digital information, processes it per a set of instructions, and provides the results. Computers found on board aircraft are used to provide vehicle and utility control; flight management; navigation, communication and identification; caution and warning; and other essential functions. The basic structure or architecture of a computer is shown in ***Figure 6-1***. It consists of a Central Processing Unit (CPU), Main Memory, and an Input and Output (I/O) system.

COMPUTER ARCHITECTURE

The Address and Data Buses provide a pathway for information to flow between the CPU, Main Memory, and the I/O system. They are referred to as parallel busses because they consist of multiple lines that send related parts of information simultaneously. Information, either data or instructions, contained on each parallel line is sent from multiple ports on the CPU to arrive at multiple ports at either the Main Memory or the I/O system, or vice versa.

The Control Bus, which provides control signals between the CPU, Main Memory, and the I/O system, is a serial bus. Buses that connect the I/O system with external input and output devices, such as displays and storage, are also serial buses. Serial buses differ from parallel buses in that one bit of information is transmitted or received one bit at a time on a single line in a serial fashion, rather than information being sent all at once over multiple lines, as is done with a parallel bus. Parallel buses tend to be short and are internal to the computer, where serial buses are used externally throughout the aircraft, as discussed in *Sub-Module 04*.

The CPU is the "brain" of the computer. It retrieves and executes instructions (i.e., sequence of steps) stored in memory and coordinates the flow of data throughout the computer in a synchronous manner controlled by the clock timing signals. The clock generates a periodic square-wave pulse train used as timing signals. Following a HIGH pulse from the clock, the CPU retrieves data and instructions from Main Memory or the I/O system on the parallel data bus, processes the data, and writes the result back on to the data bus to send to the Main Memory or to the I/O system if, for example, the result is to be displayed or put in to external storage.

The Main Memory stores the information for later access by the CPU. The Input and Output (I/O) system converts the information to other forms to facilitate communication with other onboard computers and to their operators (e.g., flight crew, technicians, etc.) through external bi-directional serial data buses, such as MIL-STD-1553B, ARINC 429, ARINC 629, etc.

BITS, BYTES, AND WORDS

Computers process information using digital data that is coded in single binary digits, known as "bits". A bit can hold 21 values, "0" and "1". Eight bits are grouped to form

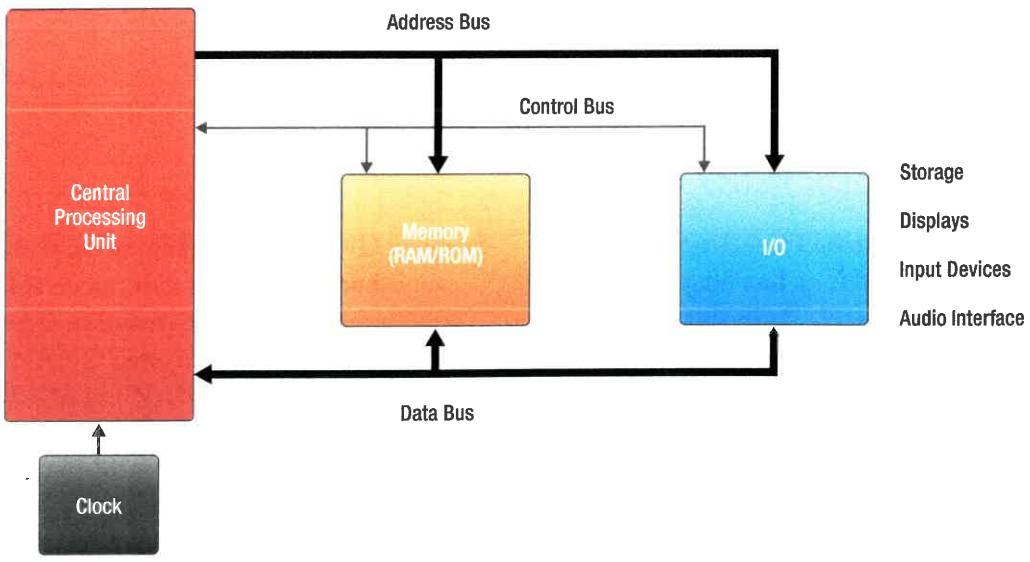


Figure 6-1. Basic computer architecture.

a "byte". A byte can hold 2^8 or 256 values. One thousand bytes, known as a Kilobyte (KB), is equivalent to the amount of information contained on a page in a book. One million bytes, or a Megabyte (MB), is equivalent to the amount of information contained in a large book. A Gigabyte (GB), or one thousand megabytes, is equivalent to the information contained in a two-hour standard-definition movie. A computer's main memory typically stores several GB of information.

1 KB = 1 000 bytes
1 MB = 1 000 KB = 1 000 000 bytes
1 GB = 1 000 MB = 1 000 000 000 bytes

Bits are grouped together to form "words". A word is a basic group of digits treated as a unit by a computer. All modern computers use a multiple of a byte as their word size. The parallel data bus between the CPU and Main Memory is normally the same width as the word size or a multiple of the word size. Thus, a 32-bit computer would typically have 32 data bus lines.

There are two types of words: instructions and data. Instructions retrieved from Main Memory tell the CPU what operation to perform on the on the data. The instructions are a series of steps, such as "branch" to a new instruction, perform a mathematical operation on the data, write the data back into Main Memory, read from the I/O system, or write to the I/O system. Branch is an instruction that may cause the computer to begin execution of a different instruction sequence.

Figure 6-2, illustrates how a 32-bit instruction word could be formed in a Reduced Instruction Set Computer (RISC). The first 6 bits are reserved for the operations code. With these 6 bits there can be 2^6 or 64 possible instructions. The remaining bits designate the destination register, source register and the immediate value. Registers (R) in the CPU provide a temporary storage area to manipulate the data as per the instruction. An immediate value is stored as part of the instruction which employs it, usually to load into, add to, or subtract from, a number stored in a register.

For example, a typical instruction might be to load the contents of memory at the value in R2, add 8, and place the result into R5. This could be followed by a second instruction to add the contents of R5 and -1, and place the result into R6. A third instruction could be to branch if the previous result is 0.

In addition to instruction words, there are data words. The numbers in the data are called operands because they are operated on by the instruction set. Operands are defined as objects of a mathematical operation. There are two basic types of data words: fixed-point and floating-point. Fixed-point data words are most common. Fixed-point is further divided into signed and unsigned data. Unsigned data is the simplest since all the bits in the data word signify the magnitude of the number.

Signed numbers are represented in two's complement form. A two's complement number can be negated (turned negative) by taking the complement of the number and then adding one. For example, bits 111 as an unsigned value would be -1 as a two's-complement value, because 111 would be complemented to 000 and adding one would result in decimal -1 as negated. Likewise, bits 110 as an unsigned value would be -2 as a two's-complement value, bits 101 as an unsigned value would be -3 as a two's-complement value, etc. A 32-bit two's complement signed number can hold values from $-2_{31}-1$ to 2_{31}. As shown in ***Figure 6-3***, for signed data, the first bit is the sign, whereby logic 0 is plus (+) and logic 1 is minus (-). The remaining bits signify the magnitude of the number. Floating-point data words are used for numbers that need to be expressed in scientific notation. After the sign bit, the 8 bits that follow are used to express the exponent with the remaining 23 bits reserved for the multiplier, as shown in ***Figure 6-4***.

SOFTWARE

Software, unlike hardware, is not a physical entity that can be touched. Instead, software specifies the operations to be performed on data. Data is used as operands by the computer instructions. Instructions can reside in either programs or in algorithms. Think of programs as arithmetic and logic operations described as a sequence of steps that implement an algorithm.

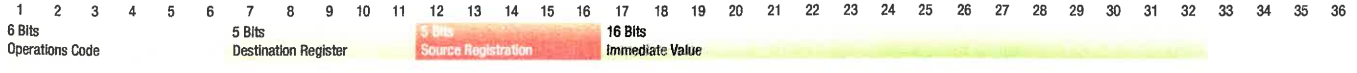


Figure 6-2. 32-bit instruction word format.

Figure 6-3. 32-bit fixed-point word format.

Figure 6-4. 32-bit floating-point word format.

There or two basic types of software, system software and application software. The system software is designed to directly operate the computer hardware. The system software includes the operating system and the I/O device drivers. The operating system instructs the overall computer operation, including start-up, file management, initiating the device drivers, and providing data input and output. It manages resources and provides common services for application software programs that runs on top of the operating system, as shown in ***Figure 6-5***. The application programs provide specific functions (e.g., Microsoft Word on a Personal Computer) to the user under the supervision of the operating system.

Software programs are usually written in a high-level programming language, such as C++, which is closer to natural language, and as such, is much easier and more efficient for a programmer to write than machine language. The high-level model-based source code is then translated into executable object code (machine language) via a software program called a compiler or an interpreter. The difference is that a compiler reads the entire source code before it generates the object code, while the interpreter reads one instruction at a time, produces the object code, and executes the instruction before reading the next instruction. Compiled programs execute much faster than interpreted programs, and for this reason, are the only programs used for avionics software development. (***Figure 6-6***)

As an alternative, small compact software programs may be directly written in low-level assembly language, which is a mnemonic representation of machine language (such as using the word "sub" for subtract). Assembly language is translated into machine language using a software program called an assembler. A high-level software command may include several assembly language instructions.

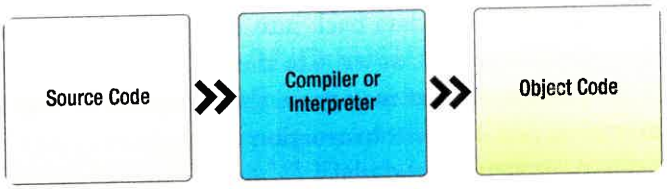


Figure 6-6. High-level source code converted in to object code (machine language).

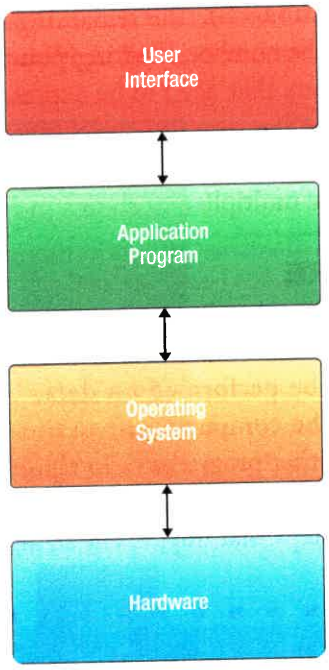


Figure 6-5. Application programs run on top of the operating system.

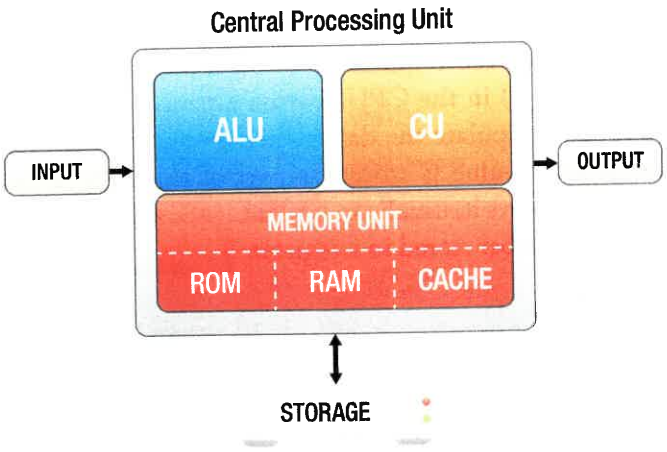


Figure 6-7. Components of the Central Processing Unit.

HARDWARE

Figure 6-7, illustrates what is known as the John von Neumann architecture after its discoverer who was the first to present the idea of stored program computers. It consists of a Central Processing Unit (CPU), which contains the Arithmetic Logic Unit (ALU), Control Unit (CU), and Main Memory Unit. It typically interfaces to external secondary memory storage and to input and output devices (called peripherals), such as a keyboard, mouse, display, printer, etc.

CENTRAL PROCESSING UNIT

A CPU microprocessor, such as the Intel Pentium 4 (*Figure 6-8*), retrieves and processes instructions and coordinates the flow of data throughout the computer. It performs math and logic calculations and sends data to and retrieves data from memory and other storage devices. The CPU contains registers, an Arithmetic Logic Unit (ALU), and a Control Unit (CU). The registers provide a temporary storage area to manipulate data during computations. The ALU combines values from the registers, such as adding numbers from different registers, and enters new values in to the registers. Most computer operations are executed in the ALU. The Control Unit (CU), supervises overall CPU operations, controls the ALU, initiates I/O functions, and decodes instructions to determine whether to add, subtract, multiply, divide, compare, or some other operation. The CU directs the data path between the registers and the ALU to perform a sequence of operations, such as moving an integer from a register to the ALU to execute a given instruction. The CU ensures that an operation is not initiated until the preceding operation is completed.

To execute an instruction, the CPU divides the action to be performed into a sequence of basic steps such that each step will be completed in one clock cycle. The higher the clock speed, the more instructions the computer can execute in any given amount of time. CPU speeds are measured in cycles per second, known as Hertz or Hz. One cycle represents a single task executed, such as adding together two numbers. Computer clock speeds are measured in Gigahertz (GHz), or one billion (10^9) cycles per second. The widely used Intel Pentium 4 runs at clock speeds of 1.3 GHz to 3.8 GHz.

Figure 6-8. Intel Pentium 4 32-bit microprocessor.

MEMORY (RAM, ROM, PROM)

Computer programs and data are stored in memory as coded binary digits (bits). There are two basic types of main memory, Random-Access Memory (RAM) and Read-Only Memory (ROM). The CPU can "randomly" add or remove data from RAM. As such, RAM is typically faster than ROM. The data portion of programs must reside in RAM during their execution. Because of the increased speed of RAM, the instruction portion of most programs is also in RAM. This is different from Read-Only Memory (ROM), which permanently stores data that can't be changed via "random" writes by the CPU. ROM keeps the data stored even after the power has been removed, thus it is termed non-volatile memory. In addition, the CPU has contained within its chip a small RAM cache storage area for frequently used data. The CPU will always access its internal cache memory before retrieving additional data from the main memory or secondary (external storage) memory.

True ROM chips are manufactured with object code stored on the chip. This is known as firmware. A variation of ROM are Programmable Read-Only Memory (PROM) chips that are manufactured blank with no instruction sets. PROMs are programmed after manufacture by plugging them into a PROM programmer where setting of each bit is locked. An ordinary PROM can't be changed once programmed. However, an Erasable PROM (EPROM) devices, can be re-programmed in the field using ultraviolet light, and an Electrically Erasable PROM (EEPROM) can be block erased and byte-written while the computer is running. Flash memory, which is faster than EEPROM, also allows memory to be erased and reprogrammed in to blocks of memory. EEPROM and Flash are used for applications that require periodic updates, such as Operational Flight Programs (OFPs), which control the overall avionic systems operation. Other types of non-volatile memory include secondary data storage, such as rotating hard-disk drives and solid-state Flash hard drives.

INTEGRATED CIRCUITS

The CPU is essentially a microprocessor contained within an integrated circuit (IC). ICs are nothing more than many complete, digital electronic circuits constructed in the same basic location. The location is known as a chip or processor, microchip or microprocessor. TTL or CMOS circuits are miniaturized and manufactured on tiny, thin, silicon semiconductor wafers. Assemblies with billions of transistors can fit on a chip the size of a fingernail. (***Figure 6-9***) With so many transistors and logic gates, computer systems with increasingly computational power are achieved.

Integrated circuits are used in nearly every modern computing and electronic device, including the many electronic devices found on aircraft. The microscopic circuits are constructed directly on the silicon chip during manufacture and cannot be removed or separated. A microprocessor contains one (or more) integrated circuit microchips at the core of the processing unit. It responds to inputs in accordance with instructions contained in its own memory. Due to the physical limitations of placing integrated circuits on a single chip, electronic developers have created microprocessors that combine the use of more than one chip in an architecture. These enable extremely fast processing due to the proximity of the integrated circuits to each on the tiny chip assemblies.

To facilitate the use of integrated circuits and other electronic components, standards have been developed. The Dual In-line Package (DIP) standard allows the installation of micro-components onto printed circuit boards. It basically calls for two rows of connecting terminals, equal-spaced along each edge of the IC housing as shown in ***Figure 6-10***. The dimensions of the terminals are standardized as is their use (e.g., power, ground, output, etc.). The come in a variety of sizes with various numbers of terminals. Inside a DIP element there can be transistor circuits, logic circuits and even complete integrated circuits and microprocessors.

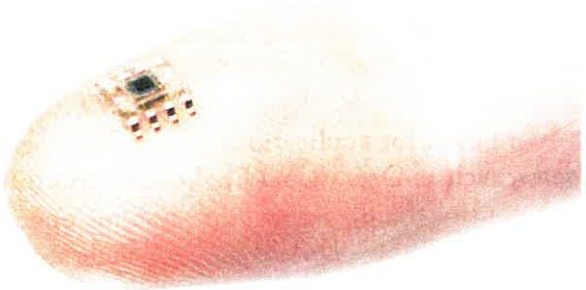


Figure 6-9. Integrated circuits.

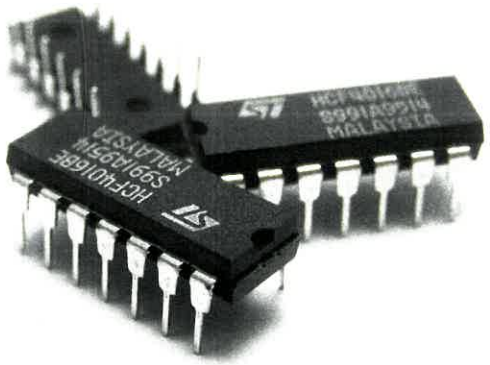


Figure 6-10. A DIP element containing a microprocessor and connection terminals for installation on a printed circuit board.

MICROCOMPUTERS

A microcomputer is nothing more than an entire computer system contained on a single printed circuit board, called a motherboard. The computer's performance, measured in Millions of Instructions per Second (MIPS), is based on its operating frequency (clock speed) and how much data is transferred per clock cycle. The higher the clock frequency, the more instructions can be executed in any given amount of time. Also, the larger the word size, the more data can be transferred during any one cycle. Thus, a 32-bit word can transfer four times the amount of data than an 8-bit word in the same clock cycle time.

LAYOUT AND INTERFACE

Figure 6-11 provides an illustration of a microcomputer with a 32-bit microprocessor (CPU) and 128K of cache memory. This particular example also contains video graphics processors to drive the displays, and controllers for main memory that is located external to the motherboard. In addition, it contains I/O controllers (device drivers) that interface with various peripherals (e.g. displays, keyboard, mouse, speakers, etc.), and in this case, an interface for secondary data storage (e.g., Secure Digital (SD) non-volatile memory card). Power supply components are located in a separate section of the microcomputer to prevent electro-magnetic interference (EMI) from adversely impacting its operations.

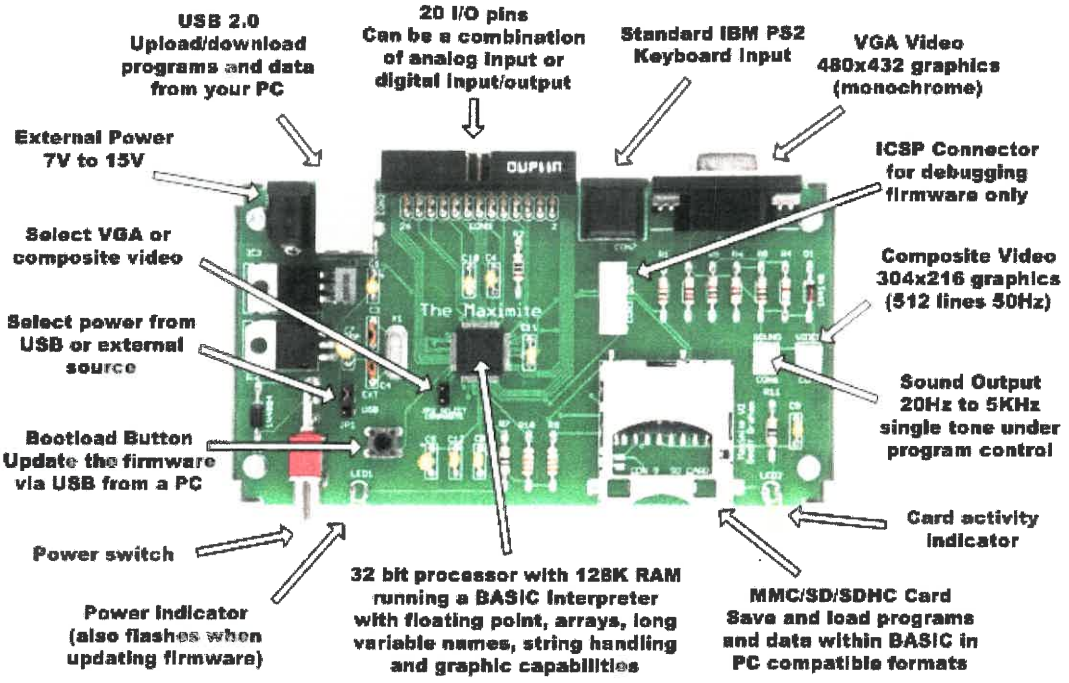


Figure 6-11. Example of a microcomputer motherboard.

OPERATION

Once power is applied to the microcomputer, a software program stored in ROM called the Basic Input/Output System (BIOS), performs a power-on self-test, sets up the I/O ports, and loads the operating system software, configuration files, and batch files into main memory. BIOS provides a common control interface between the operating system and the various application programs. Once an application program is executed, the results are stored in memory as input to another program, or sent externally through the I/O system. For example, at the beginning of an operation, an instruction could be read from an input device, such as a keypad, and written (stored) into main memory. After storage is complete and the program is executed, the results are read from memory and sent to an output device, such as a display.

Referring to ***Figure 6-12***, when a computer needs to perform an operation, the processor will initiate a read or write cycle and specify a memory location over the Address Bus. The RAM Memory Controller then locates the memory address and the processor issues a signal over the Control Bus indicating the cycle type as either a memory "read" or a memory "write". For a memory write cycle, the processor writes the data from its internal registers into the specified memory address and sends it along the Data Bus to store in memory. The cycle is concluded when the RAM Memory Controller sends a "ready" signal back to the processor over the Control Bus signifying the operation is complete. For simplicity, all three buses, address, data, and control are referred to as the "System Bus".

After the operation has been completed, another cycle begins whereby the processor initiates a read cycle and specifies the memory location over the Address Bus. The control unit causes the data to be read from memory and program instructions to be executed in the arithmetic logic unit. Once the program has been executed, the control unit causes the results to be read from main memory and sent to an output device, such as a cockpit display.

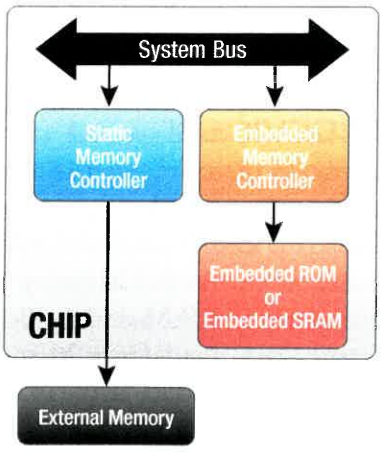


Figure 6-12. Microcomputer operations.

In the event that an I/O device requires urgent servicing, the I/O device will send an interrupt signal through the Control Bus to the processor, which may cause it to temporarily postpone executing its current instructions, depending on the system status. If the processor determines that the interrupt is more important than the current task being performed, it will store its current state in to a designated memory address location.

However, once the interrupt request has been serviced, the processor will access the partially completed operation from its designated memory access location and complete the execution of the original operation. An Interrupt Controller is often used to prioritize the myriad of interrupts that can be generated by each of the I/O device controllers.

INSTRUCTION WORDS

Instruction words tell the computer what operation to perform on the data. Each word has a distinct memory address location assigned to it. The most commonly used set of instruction words, as illustrated in ***Figure 6-13***, are as follows:

- Data Transfer – used for reading or writing data, setting a register to a fixed constant value, and loading and storing data to a memory location from a register or vice versa.
- ALU Operations – used for adding, subtracting, multiplying or dividing the values of two registers, comparing two values in a register, or complicated integer and Floating-Point (FP) arithmetic (e.g., sine, cosine, square root, etc.)
- Control Transfer – used for controlling operations, such as branching to another register location in the program and executing instructions in the new location; or perhaps for manipulating multiple bytes of data (called strings) in order to save data contained on many registers on the stack at once.

MEMORY DEVICES

As stated previously, there are two basic types of main memory, Random-Access Memory and Read-Only Memory. The CPU can "randomly" add or remove data from the Random-Access Memory (RAM) and programs must reside in RAM during their execution. This is different from Read-Only Memory (ROM), which permanently stores data that can't be changed. ROM and variations of ROM, such as PROM and EPROM, keeps the data stored even after the power

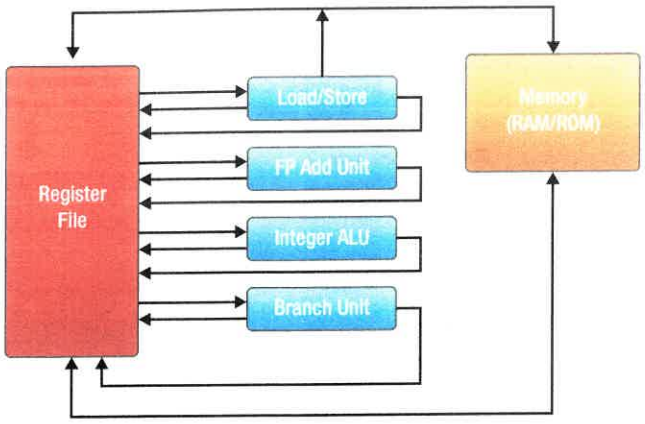


Figure 6-13. Typical instruction words.

has been removed, thus it is called non-volatile memory. Other types of non-volatile memory include external secondary data storage, such as hard-disk drives and solid-state Flash memory.

There are two basic types of RAM memory devices: Static RAM (SRAM) and Dynamic RAM (DRAM). SRAM is used for high-speed direct-access cache memory. SRAM is located within the same chip as the CPU microprocessor and is optimized to run at the same speed as the CPU. DRAM is the main memory used for indirect access and it typically located on a separate PCB (printed circuit board) that connects into the motherboard, as shown in ***Figure 6-14***.

DRAM contains only one transistor per bit providing more memory at a higher density and a lower cost compared to SRAM which typically has 4 to 6 transistors per bit. However, DRAM is much slower than SRAM. So why does a micro-computer need both SRAM and DRAM? Think of SRAM cache memory as a refrigerator and DRAM main memory as a grocery story. One will go directly to the refrigerator to obtain food as it provides quick and easy access due to its close

Figure 6-14. Typical DRAM data storage PCB.

proximity. However, when the refrigerator is low on food, a trip is needed to the grocery store to replenish the supplies.

All though the grocery store is not nearly as convenient as the refrigerator, it can store an abundance. The same can be said about the DRAM main memory.

Let's examine the memory management process using this analogy. When the CPU issues a read cycle to fetch data from main memory, the cache controller will intercept the request and check its directory address tags to see if it contains the data. If not, the request is sent to the main memory where the DRAM controller will send the requested data to the CPU with a copy stored in cache. The next time the CPU requests the data, the cache controller will disrupt the request from being sent to main memory since it can provide the data directly to the CPU much faster than having to access the data again from the main memory. (***Figure 6-15***)

The cache controller keeps track of when data was last accessed by the CPU so that old data in the cache is continually replaced by newer data. The cache controller also monitors the data bus to make certain that the data contained in cache is the very latest version of the data stored in main memory. If the cache controller determines a newer version of data exists in main memory, it will halt sending invalid data to the CPU, but instead, will allow the request to be sent to the DRAM controller so that the CPU and its cache memory will have the very latest data from which to execute the program instructions.

DATA STORAGE SYSTEMS

Data storage systems are external memory devices that store large amount of application data and program instructions that are available to be downloaded in to main memory via an external serial data bus. Using the previous analogy, think of secondary data storage systems as the warehouse for the grocery store. There are two basic types of non-volatile data storage systems, solid-state memory (e.g., flash memory) and hard compact disc or optical drives.

Figure 6-16 is an illustration of a hard-disc drive commonly used in computer systems for providing external data storage. The amount of storage is determined by the size of the disc, which can be either 5", 3.5" or 2.5".

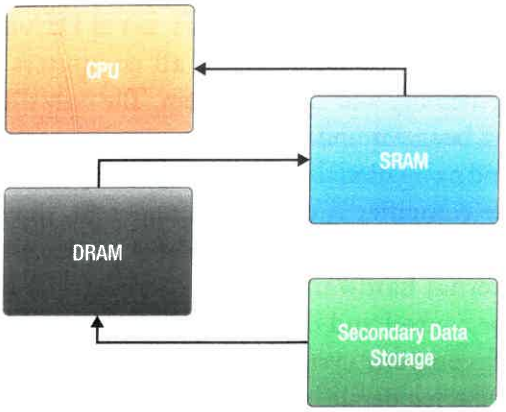


Figure 6-15. Memory management process.

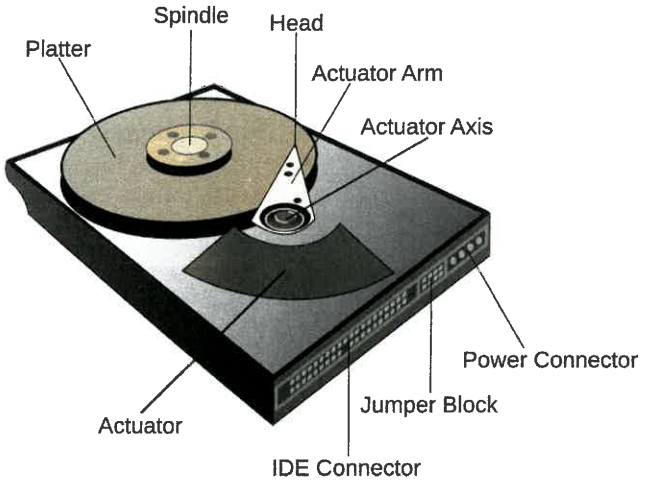


Figure 6-16. Hard-disc drive data storage system.

The access time is determined by the time it takes the play head to find the location of the data on the disc plus the rotation speed of the disc, typically between 4 200 RPM and 15 000 RPM.

The transfer of large amounts of data, including application programs, from external secondary memory storage to RAM main memory can be performed by the CPU; however, doing so prevents the processor from performing other important operations. Therefore, a Direct Memory Access (DMA) controller, located on the motherboard, is used free up the processor during bulk data transfer. The CPU sends an instruction to the DMA controller to transfer a specified block of data to or from a specific memory location over a serial bus, and the DMA controller responds when the data transfer has been completed. DMA transfer is faster and more efficient than having the CPU conduct the data transfer operation.

AIRCRAFT COMPUTER SYSTEMS

Regardless of the application, all computers have a CPU, a memory and an I/O system. The only difference between business and personal computers and aircraft flight and navigational computers lies in the environment that the computer is designed to operate, the type of external serial data bus system that it interfaces to, and the external hardware devices (peripherals) that are used for control and display of the computer systems. Aircraft computer systems must be designed to operate in extreme temperate, acceleration, vibration, shock and EMI environments that would not be encountered in a controlled office setting. Also, flight-critical aircraft computer systems must be certified to be fail-safe, such that hardware or software errors can't cause a catastrophic safety-of-flight incident.

Typical peripherals for a Flight Management Computer (FMC) are cockpit displays, an external secondary data storage device, and a Control and Display Unit (CDU). The external secondary data storage device is known as a Data Transfer System (DTS). It is used for uploading navigation flight plans to the FMC and for downloading maintenance data. A CDU is a keyboard input device with a small display located in the cockpit center console for entering and retrieving flight management information. As shown in ***Figure 6-17***, most aircraft will have two CDUs and two FMCs for redundancy purposes, so if one system fails, the crew will always have a back-up. The FMC shown on the right has four printed circuit boards: CPU motherboard, DRAM mass memory board, I/O board, and an EMI-shielded power supply board. The complete operation of Flight Management Systems (FMS) will be discussed in greater detail in *Sub-Module 15*.

Figure 6-17. Typical aircraft computer system used for flight management.

Question: 6-1
What are the three basic components of a computer and what are their functions?

Question: 6-2
Explain the differences between serial data buses and parallel data buses.

Question: 6-3
What are instruction words?

Question: 6-4
What function does the system software perform?

Question: 6-5
What is the difference between a compiler and an interpreter?

Question: 6-6
What are the three main components of a Central Processing Unit (CPU) and what functions does each of these components perform?

Question: 6-7
Explain the difference between Random-Access Memory (RAM) and Read-Only Memory (ROM).

Question: 6-8
What is an Integrated Circuit (IC)?

ANSWERS

Answer: 6-1
The basic structure of a computer consists of a Central Processing Unit (CPU), Main Memory, and an Input and Output (I/O) system. The CPU is the "brain" of the computer. It retrieves and executes instructions stored in memory and coordinates the flow of data throughout the computer in a synchronous manner controlled by the clock timing signals. The Main Memory stores the information for later access by the CPU. The I/O system facilitates communication with other onboard computers and to their operators through external serial data buses.

Answer: 6-2
Serial buses differ from parallel buses in that one bit of information is transmitted or received one bit at a time on a single line in a serial fashion, rather than information being sent all at once over multiple lines, as is done with a parallel bus. Parallel buses tend to be short and are internal to the computer, where most serial data buses are external to the computer. Buses that connect the I/O system with external input and output devices, such as displays and storage, are serial buses.

Answer: 6-3
Instructions words retrieved from Main Memory tell the CPU what operation to perform on the data. The instructions are a series of steps such as "branch" to a new instruction, perform a mathematical operation on the data, write the data back into Main Memory, read from the I/O system or write to the I/O system.

Answer: 6-4
The system software is designed to directly operate the computer hardware. The system software includes the operating system and the I/O device drivers. The operating system instructs the overall computer operation, including start-up, file management, initiating the device drivers, and providing data input and output. It manages resources and provides common services for application software programs that run on top of the operating system.

Answer: 6-5
The difference is that a compiler reads the entire source code before it generates the object code, while the interpreter reads one instruction at a time, produces the object code, and executes the instruction before reading the next instruction. Compiled programs execute much faster than interpreted programs, and for this reason, are the only programs used for avionics software development.

Answer: 6-6
The CPU contains registers, an Arithmetic Logic Unit (ALU), and a Control Unit (CU). The registers provide a temporary storage area to manipulate data during computations. The ALU combines values from the registers, such as adding numbers from different registers, and enters new values in to the registers. The Control Unit, supervises overall CPU operations, controls the ALU, initiates I/O functions, and decodes instructions to determine whether to add, subtract, multiply, divide, compare, or some other operation.

Answer: 6-7
RAM is typically faster than ROM because the CPU can randomly add or remove data from RAM. Because of its increased speed, the instruction portion of most programs is also in RAM. This is different from ROM, which permanently stores data that can't be changed via random writes by the CPU. ROM keeps the data stored even after the power has been removed, thus it is termed non-volatile memory.

Answer: 6-8
ICs are nothing more than many complete, digital electronic circuits constructed in the same basic location. The location is known as a chip or processor, microchip or microprocessor. A CPU is essentially a microprocessor contained within an IC.

Question: 6-9
What determines the performance of a computer and how is it measured?

Question: 6-10
What is the function of the Basic Input/Output System (BIOS)?

Question: 6-11
Explain the operation of a RAM Memory Controller during a "write" cycle.

Question: 6-12
What is the purpose of an Interrupt Controller?

Question: 6-13
Name the three most common types of Instruction Words.

Question: 6-14
What is the difference between Static-RAM (SRAM) and Dynamic-RAM (DRAM)?

Question: 6-15
Explain the operation of the Cache Controller.

Question: 6-16
What function does the Direct Memory Access (DMA) controller perform?

ANSWERS

Answer: 6-9
A computer's performance, measured in Millions of Instructions per Second (MIPS), is based on its operating frequency (clock speed) and how much data is transferred per clock cycle. The higher the clock frequency, the more instructions can be executed in any given amount of time. Also, the larger the word size, the more data can be transferred during any one cycle.

Answer: 6-10
For an AND gate to have a Logic 1 output, all inputs have to be Logic 1. In an actual electronic circuit, this means that for a voltage to be present at the output, the AND gate circuit has to receive voltage at all of its inputs.

Answer: 6-11
The RAM Memory Controller locates the memory address so the processor can write the data from its internal registers into the specified memory location. When the operation is complete, the RAM Memory Controller sends a "ready" signal back to the processor.

Answer: 6-12
In the event that an I/O device requires urgent servicing, the I/O device will send an interrupt signal through the Control Bus to the processor, which may cause it to temporarily postpone executing its current instructions. An Interrupt Controller is used to prioritize the myriad of interrupts that can be generated by each of the I/O device controllers.

Answer: 6-13
Data Transfer, ALU Operations, and Control Transfer.

Answer: 6-14
SRAM is used for high-speed direct-access cache memory. SRAM is located within the same chip as the CPU microprocessor and is optimized to run at the same speed as the CPU. DRAM provides more memory at a higher density and a lower cost compared to SRAM and is used for Main Memory applications.

Answer: 6-15
When the CPU issues a read cycle to fetch data from main memory, the Cache Controller will intercept the request and check its directory address tags to see if it contains the data. If not, the request is sent to the main memory where the DRAM controller will send the requested data to the CPU with a copy stored in cache. The next time the CPU requests the data, the Cache Controller will disrupt the request from being sent to main memory since it can provide the data directly to the CPU much faster than having to access the data again from the main memory.

Answer: 6-16
A DMA controller frees up the processor during bulk data transfer. The CPU sends an instruction to the DMA controller to transfer a specified block of data to or from a specific memory location over a serial bus, and the DMA controller responds when the data transfer has been completed.

DIGITAL TECHNIQUES ELECTRONIC INSTRUMENT SYSTEMS

MICROPROCESSORS

SUB-MODULE 07

PART-66 SYLLABUS LEVELS

CERTIFICATION CATEGORY → B2

Sub-Module 07

MICROPROCESSORS

Knowledge Requirements

5.7 - Microprocessors

Functions performed and overall operation of a microprocessor;	2
Basic operation of each of the following microprocessor elements: control and processing unit, clock, register, arithmetic logic unit.	

5.7 - MICROPROCESSORS

As previously stated, a microprocessor is nothing more than a Central Processing Unit (CPU) contained on a single integrated circuit (IC or "chip"). The microprocessor is essentially the "brains" of the computer that interfaces with the memory and I/O devices. It retrieves and processes instructions and coordinates the flow of data throughout the computer. It performs math and logic calculations and sends data to/from memory and other storage devices.

The Boeing 777 uses 32-bit Motorola MC68000 chips running at clock speeds of 20 Mhz. ***Figure 7-1*** (left) is a MC68000 wafer die with feature sizes shown as small as 3.5 microns (a micron is one millionth of a meter). On the right, is the microprocessor wafer die mounted on a lead frame package ready to plug into a receptacle socket on the motherboard.

FUNCTIONS PERFORMED

The pins protruding from a typical micro-processor are for performing the following functions:

- Clock Input – provides timing for the microprocessor so that it can execute instructions.
- Data Bus – carries bits of information between the microprocessor and other devices. A single-core 32-bit processor has 32 pins since it communicates over a 32-bit parallel data bus.
- Control Bus – signals that indicate the beginning and end of each microprocessor cycle.
- Address Bus – contains the location of the information that the microprocessor needs to access or modify. The number of address lines determines the number of register locations. A processor with 20 address lines can access 2^{20} (one million) locations.
- Interrupt Input – an urgent request for service. For example, a keyboard stroke or a bit parity error would cause an interrupt signal to be sent to the microprocessor causing it to temporarily postpone executing its current instructions.
- Address Latch Enable – indicates which bytes on the address bus are valid to use.
- Bus Arbitration – tells the microprocessor that another controller wants access to the bus. When the bus is free, the microprocessor will output a "hold acknowledge" signal allowing the controller to send its request for service.
- Status Signals – indicates the type of cycle being run. For example, a write/read signal indicates whether the microprocessor is sending data or requesting data, and a memory I/O signal indicates whether the cycle is intended for main memory or for an I/O device.
- Voltage and Ground – either 5 volts DC for TTL logic or 3.3 volts DC for CMOS logic.

OVERALL OPERATION

FUNCTIONAL COMPONENTS

Figure 7-2 illustrates the functional components of the Pentium 32-bit microprocessor. The Pentium chip contains a dual-core processor allowing two 32-bit instruction sets to be run simultaneously, transferring data over an internal 64-bit bus from cache memory to the bus interface unit. At the core of the microprocessor are two Arithmetic Logic Units (ALU) that execute

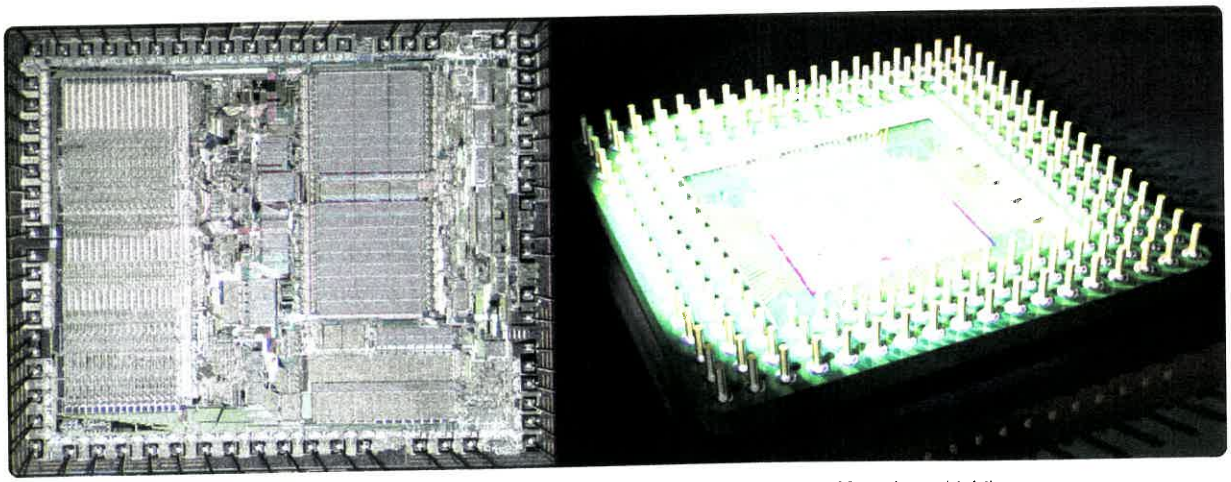


Figure 7-1. MC6800 microprocessor wafer die (left) mounted in its IC package (right).

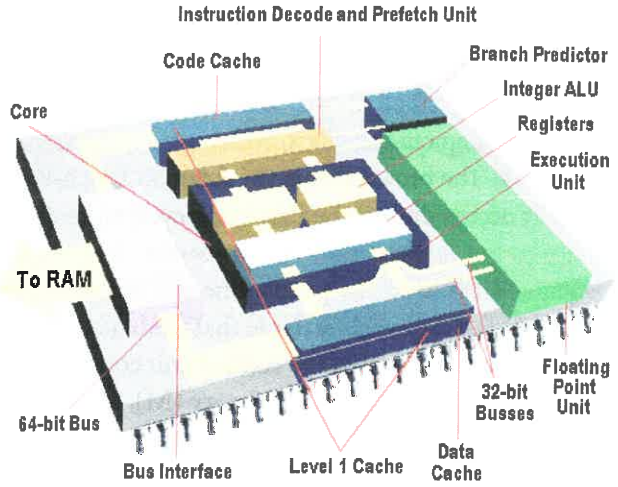


Figure 7-2. Microprocessor functional components.

all the arithmetic (e.g., add, subtract, multiply, divide, shift) and logic (e.g., NOT, AND, NAND, OR, XOR) operations specified by the instruction sets. It also has a floating point unit, called a math coprocessor, to handle complex computations. (e.g., sine, cosine, square root).

Besides the dual ALUs, the core execution unit contains registers and the control unit. Registers provide small fast memory locations for the temporary storage of values used in computations. Data residing in the registers can be accessed quickly without running external bus cycles to cache or main memory, thereby improving execution time. The ALUs combine values from the registers, such as adding or subtracting numbers from different registers, and enters new values in to the registers. A 32-bit microprocessor typically has a 32-bit register to accommodate a 32-bit addressable location in cache or main memory.

The control unit contains the microprocessor's microcode, which are low-level commands permanently stored in ROM inside the microprocessor. As such, the control unit supervises overall CPU operations, controls the ALU, initiates I/O functions, and decodes instructions to determine whether to add, subtract, multiply, divide, compare, or some other operation. The control unit directs the data path between the registers and the ALU to perform a sequence of operations, such as moving an integer from a register to the ALU to execute a given instruction. Finally, the control unit ensures that an operation is not initiated until the preceding operation is completed. All computer operations, including synchronization of I/O transfers with the clock timing signals, are controlled by the control unit.

Outside the core are the instruction prefetch and decode unit and the branch predictor, both of which are used to make the microprocessor run more efficiently. The prefetch and decode unit is responsible for keeping the microprocessor busy processing instructions and data. When the bus interface unit is not running bus cycles to execute an instruction, the prefetch unit uses the bus unit to sequentially fetch the next few instructions, which are then stored in a prefetch queue. The decode unit takes the instructions stored in the prefetch queue, decodes them, and then stores them in an instruction queue until requested by the control unit. This increases performance so that the ALU doesn't have to wait for the next instruction set.

The branch predictor monitors the flow of instructions to and from specified memory branches and stores a record of previously executed instructions in a small cache called a branch target buffer. In particular, it looks at what causes a branch to occur in the normal sequential flow of instructions and uses this information to predict the outcome of future branches so as to alter the instruction execution sequence. The branch prediction is correct most of the time, which results in up to a 25% increase in performance.

Microprocessors track information using logical addresses. As such, microprocessors typically have a Memory Management Unit (MMU), also known as a segmentation and paging unit, which translates each logical address into a physical address that corresponds with a specified location in main memory. (***Figure 7-3***)

The MMU assists the operating system by creating a simplified addressing environment for running simultaneous application programs without having the programs interfere with each other. It does this by giving

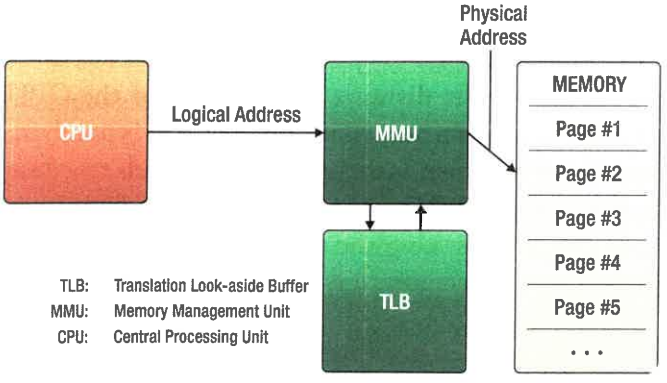


Figure 7-3. Memory management unit.

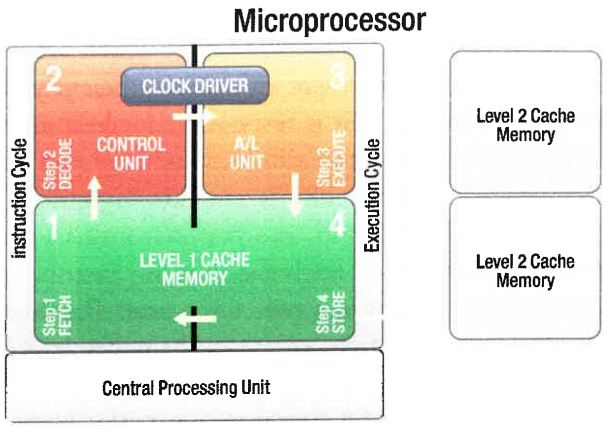


Figure 7-4. Microprocessor basic operation.

each program its own unique address segment location and then partitioning main memory into 4 kilobyte pages to support a virtual memory environment where large address spaces are simulated using a small amount of DRAM or hard-disc drive storage.

MACHINE CYCLE

Figure 7-4 illustrates the basic operation of a microprocessor. To execute an instruction, the CPU divides the action to be performed into a sequence of basic steps such that each step will be completed in one clock cycle. The higher the clock driver speed, the more instructions the computer can execute in any given amount of time. To begin an operation, the control unit will fetch program instructions from cache memory and then decode the instructions, which may also require fetching data from memory. The ALU then executes these instructions and stores the results back into cache memory. These four steps (fetch, decode, execute, and store) make up one microprocessor "machine" cycle.

It is worthwhile to mention that there may exist different levels of cache memory. Level 1 cache is located on the chip for high-speed direct access. Whereas Level 2 cache is positioned external of the chip, but adjacent to it, to provide additional direct memory access, albeit slower due to the distance between it and the CPU. Whenever the data needed by the processor is not found in cache, it is known as cache "miss", and leads to a delay in execution by having to retrieve the data from main memory, thus making the system slow. If the data is found in cache memory, it is known as cache "hit".

CLOCK TIMING

Figure 7-5 is a timing diagram used to illustrate the "fetch" step described above. The red line on the top of the diagram depicts the clock cycles used to execute the instructions. The brown line is the Address Latch Enable (ALE). It occurs during the first clock cycle to enable the address to get latched into the processor. The memory location address is on the purple line and the data frame retrieved is on the green line. Note that the blue and yellow status signals indicate that the control unit command is to read (RD) the data into main memory (M).

In order to increase processor speed and efficiency, instructions are often processed in parallel by the various functional components in the microprocessor, each at a different stage of execution, as shown in ***Figure 7-6***. This is known as parallel processing or instruction pipelining.

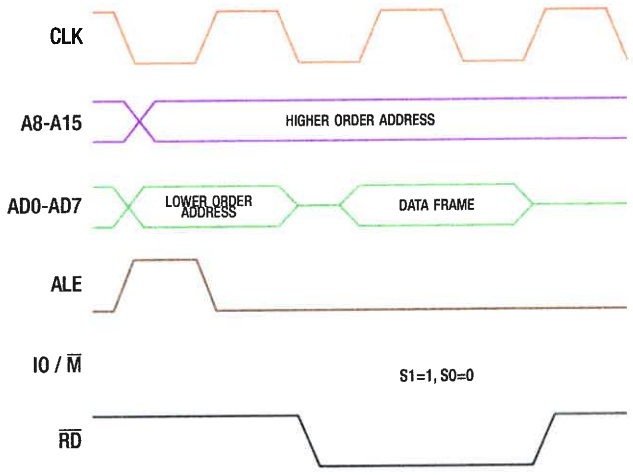


Figure 7-5. Timing signal example.

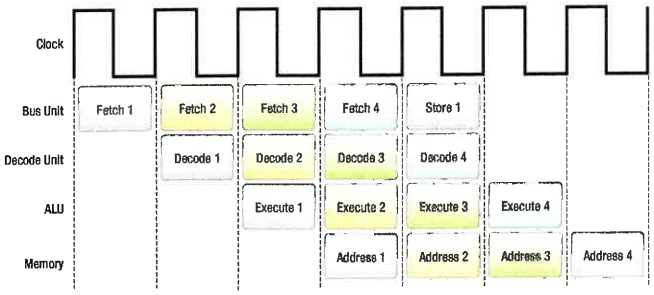


Figure 7-6. Instruction pipelining.

Question: 7-1
Explain the function of the Data Bus, Control Bus, and Address Bus.

Question: 7-2
Name two types of status signals that could be sent by a microprocessor.

Question: 7-3
A core execution unit contains one or more ALUs, Registers and the Control Unit. What is purpose do the Registers serve.

Question: 7-4
Explain the purpose of the Control Unit.

Question: 7-5
How does Prefetch and Decode unit make microprocessor more efficient?

Question: 7-6
What is the purpose of the Branch Predictor?

Question: 7-7
How does the Memory Management Unit (MMU) assist the Operating System?

Question: 7-8
What are the four basic steps that make up one microprocessor "machine" cycle?

ANSWERS

Answer: 7-1
The Data Bus carries bits of information between the microprocessor and other devices. The Control Bus provides signals that indicate the beginning and end of each microprocessor cycle. Address Bus contains the location of the information that the microprocessor needs to access or modify. The number of address lines on the bus determines the number of register locations.

Answer: 7-2
A write/read signal indicates whether the microprocessor is sending data or requesting data. A memory I/O signal indicates whether the cycle is intended for main memory or for an I/O device.

Answer: 7-3
Registers provide small fast memory locations for the temporary storage of values used in computations. Data residing in the registers can be accessed quickly without running external bus cycles to cache or main memory, thereby improving execution time. The ALUs combine values from the registers, such as adding or subtracting numbers from different registers, and enters new values in to the registers.

Answer: 7-4
The control unit supervises overall CPU operations, controls the ALU, initiates I/O functions, and decodes instructions to determine whether to add, subtract, multiply, divide, compare, or some other operation. The control unit directs the data path between the registers and the ALU to perform a sequence of operations, such as moving an integer from a register to the ALU to execute a given instruction.

Answer: 7-5
When the bus interface unit is not running bus cycles to execute an instruction, the prefetch unit uses the bus unit to sequentially fetch the next few instructions, which are then stored in a prefetch queue. The decode unit takes the instructions stored in the prefetch queue, decodes them, and then stores them in an instruction queue until requested by the control unit. This increases performance so that the ALU doesn't have to wait for the next instruction set.

Answer: 7-6
The branch predictor monitors the flow of instructions to and from specified memory branches and stores a record of previously executed instructions in a small cache called a branch target buffer. In particular, it looks at what causes a branch to occur in the normal sequential flow of instructions and uses this information to predict the outcome of future branches so as to alter the instruction execution sequence.

Answer: 7-7
The MMU assists the operating system by creating a simplified addressing environment for running simultaneous application programs without having the programs interfere with each other. Applications share a common logical address space, but are mapped to different physical addresses.

Answer: 7-8
To begin an operation, the control unit will fetch program instructions from cache memory and then decode the instructions, which may also require fetching data from memory. The ALU then executes these instructions and stores the results back into cache memory. These four steps (fetch, decode, execute, and store) make up one microprocessor "machine" cycle.

PART-66 SYLLABUS LEVELS

CERTIFICATION CATEGORY → B2

Sub-Module 08

INTEGRATED CIRCUITS

Knowledge Requirements

5.8 - Integrated Circuits

Operation and use of encoders and decoders;	2
Function of encoder types;	
Uses of medium, large and very large scale integration.	

5.8 - INTEGRATED CIRCUITS

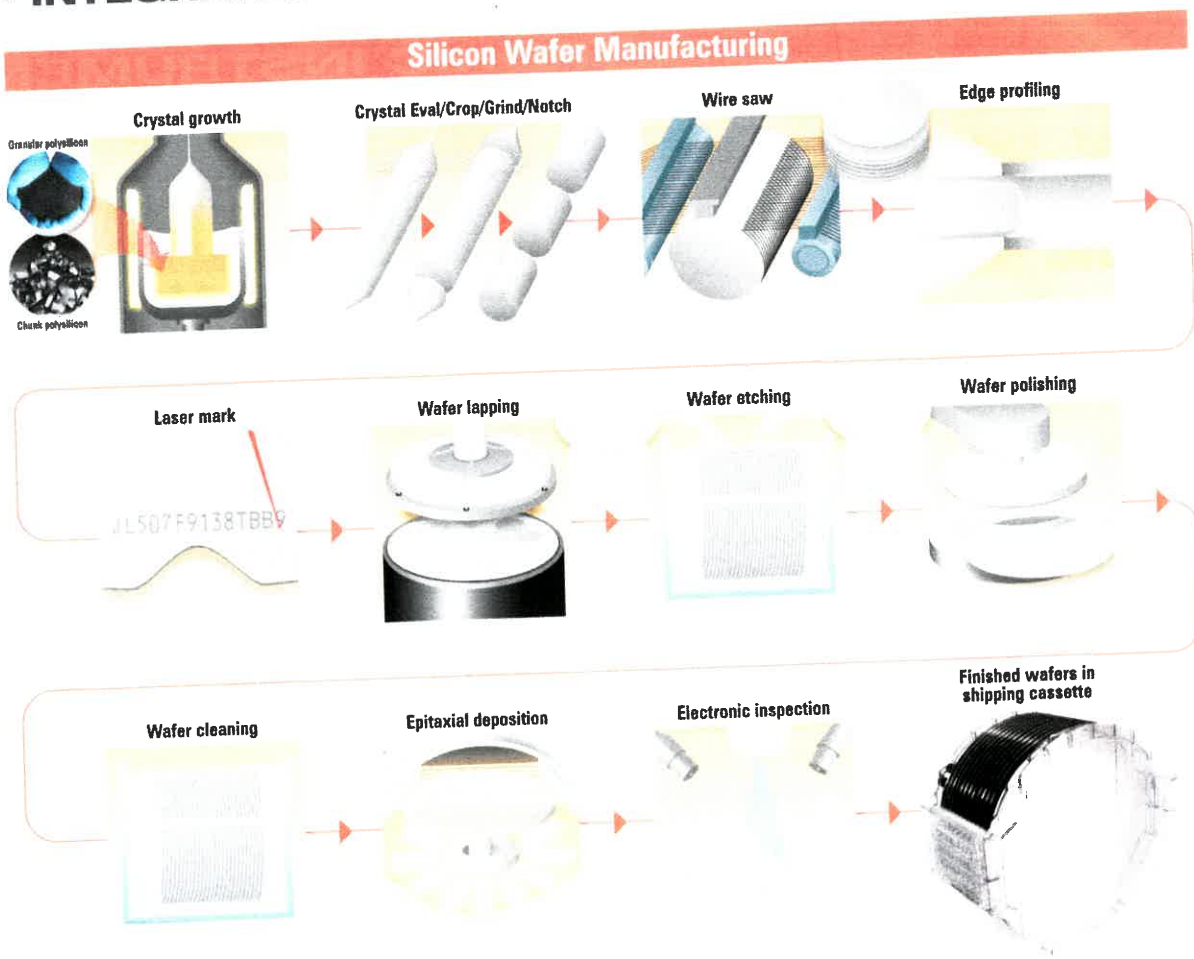


Figure 8-1. ICS's are manufactured on thin semiconductor wafers.

As previously stated, Integrated Circuits (ICs), also known as chips, are nothing more than miniaturized electronic circuits that contain over a million tiny electronic components. Chips are manufactured from a wafer of a thin substrate of semiconductor material, such as silicon, gallium nitride, gallium arsenide, etc.

The process begins with growing the crystal material. As shown in ***Figure 8-1***, the material is then processed in to the shape of thin round wafers. The electronic circuits are etched into the wafers using photo lithographic and chemical processing steps to form hundreds of chips. The wafers are then polished, cleaned, and inspected. The individual chips are cut from the wafers and mounted in plastic or ceramic packages. Tiny wires are soldered from the chip to the connector pins and it undergoes a final test. (***Figure 8-2***) All of the discrete components, such as resistors, transistors, diodes, and capacitors, are constructed on these small pieces of semiconductor material and are an integral part of the chip. They come in a variety of sizes with various numbers of terminals. Inside there can be transistor logic circuits or a complete microprocessor with cache memory and a bus interface.

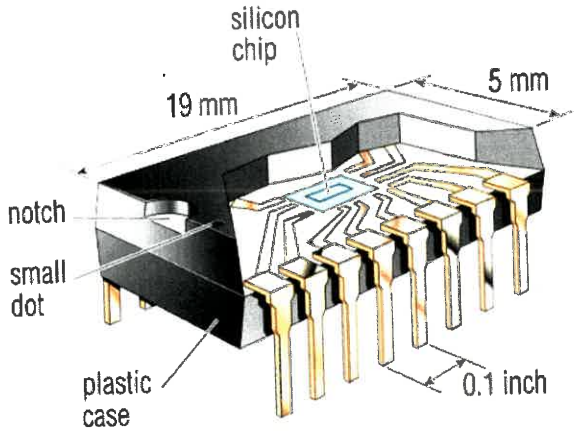
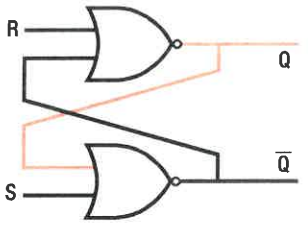


Figure 8-2. Silicon chip mounted in a dual-inline package.

Sub-Module 05 discussed logic circuit ICs, such as half and full adders. *Sub-Module 07* discussed microprocessor ICs. This *Sub-Module* will discuss other ICs used in digital electronics, such as flip-flops, comparators, encoders, and decoders. Finally, there will be a discussion on various levels or scales of chip integration and what type of circuits are contained in each level.

FLIP-FLOPS

Flip-flops are bi-stable multi-vibrator circuits that form basic storage units of sequential logic used in shift registers and counters. They have the ability to maintain their state without further application of a signal allowing them to store a bit of data or one place of a larger binary number. Their ability to set one condition and reset or change to an alternate condition results in a latch, also known as a flip-flop. Either cross-coupled NAND gates or cross-coupled NOR gates (***Figure 8-3***) are used to form Reset-Set (RS) flip-flop circuits. Each gate has two inputs and two outputs. The outputs Q and $\overline{Q}$ are always in opposite states, so if Q is set to logic 1 then $\overline{Q}$ is reset to logic 0, and vice versa.



S	R	Q	$\overline{Q}$
0	0	No Change	
0	1	0	1
1	0	1	0
1	1	disallowed	

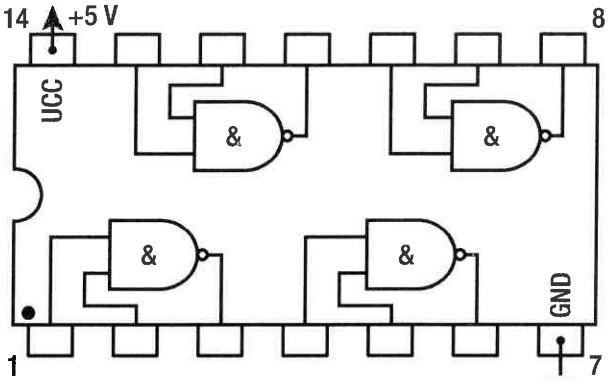
Figure 8-3. RS flip-flop using cross-coupled nor gates and its truth table.

To turn on the flip-flop circuit, the Set (S) gate receives a +5v signal which is inverted to a logic 0 and sent to the input of the Reset (R) gate. Since both inputs to the R gate are logic 0, the Q output is inverted to a logic 1 (red) which is fed to the alternate input of the S gate causing its $\overline{Q}$ output to be logic 0 (black). When both inputs are logic 0, the flip-flop remains in an unchanged (remember) state until a +5v signal is applied to either gate to reset the flip-flop. The disallowed (unused) state is when inputs to both the R and S gates are logic 1.

The truth table for the cross-coupled NAND RS flip-flop is exactly the same as the NOR RS flip-flop, except that if both inputs are logic 1, the flip-flop is in a remember state, and having both inputs as logic 0 is disallowed.

Figure 8-4 is a picture of a 7400 chip in a DIP package containing four NAND gates, which is sufficient to form two RS flip-flop circuits. The two additional pins, VCC and GND, are for +5v power and ground respectively.

When using flip-flops, it is often desirable to establish the logic level outputs at a time other than when the signals are initially applied. This is accomplished using a flip-flop circuit that is triggered by a clock input. The clock pulse acts as the control to allow the signals that



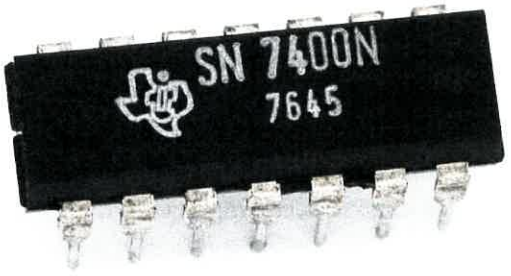


Figure 8-4. TI 7400 NAND chip.

appears at inputs of the S and R gates to pass to the cross-coupled flip-flop. Depending on the design, either the rising edge or the trailing edge of the clock pulse can trigger the flip-flop.

Figure 8-5 illustrates a clocked RS flip-flop using NAND gates and its associated timing diagram where CLK (C) is the clock timing pulse, S and R are the inputs and Q and $\overline{Q}$ are the outputs.

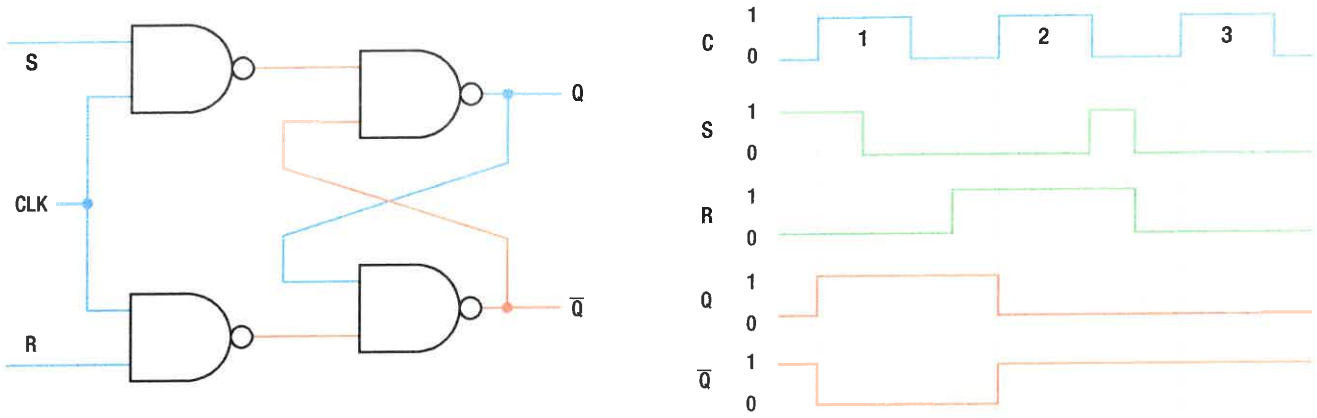


Figure 8-5. Clocked RS flip-flop using NAND gates with timing diagram.

The timing diagram shows that the rising edge of the first clock pulse sets Q to logic 1 because S is set to logic 1. Later, S changes to logic 0 and R changes to logic 1. However, Q remains set at logic 1 until the second clock pulse is detected, which resets Q to logic 0 and $\overline{Q}$ to logic 1.

A very popular logic circuit is the clocked JK flip-flop, shown in ***Figure 8-6***. The JK flip flop has the distinct advantage that they are no disallowed combinations as with the RS flip flops. When J and K are both at logic 1, the outputs Q and $\overline{Q}$ will toggle on and off with the rising edge of every clock pulse. When J = 1 and K = 0, the flip-flop will set Q to 1 and $\overline{Q}$ to 0 on the first clock pulse, if not already set to this state. When J = 0 and K = 1, Q will reset to 0 and $\overline{Q}$ will reset to 1 on the next clock pulse. When both J and K are set to 0, all clock pulses will be blocked from turning on the first two NAND gates resulting in no change occurring in either of the outputs.

COMPARATORS

Unlike a flip-flop that counts and stores binary numbers, the function of a comparator is to compare sets of binary numbers. Comparators are often used as parity checkers. An example of a comparator is the 7484 chip (***Figure 8-7***) that compares the 4 bits that are input to A to the 4 bits that are input to B and provides a signal on one of three comparison outputs depending on whether A is less (<) than B, A is equal (=) to B, or A is greater (>) than B. For example, if the binary input to A is 1010 (decimal number 10) and the binary input to B is 1101 (decimal number 13), there would be a logic 1 signal present on the output labeled A<B.

The 7485 chip has three additional inputs for cascading comparators when comparing larger binary numbers. For example, the first comparator can be used to compare units, a second comparator added to compare tens, a third comparator used to compare hundreds, etc. In the diagram shown in ***Figure 8-8***, the left 7485 chip, used for comparing tens, is cascaded to the right 7585 chip, used for comparing units.

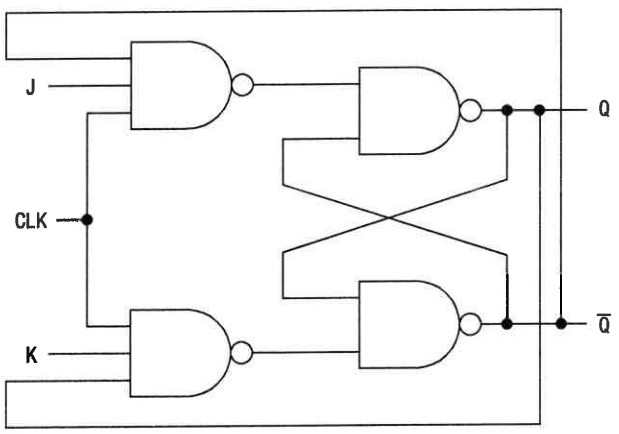


Figure 8-6. JK flip-flop using NAND Gates.

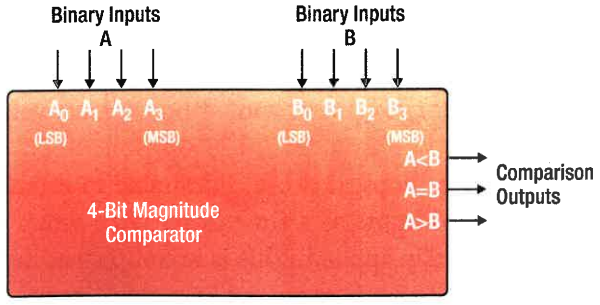


Figure 8-7. 7485 chip (4-bit magnitude comparator).

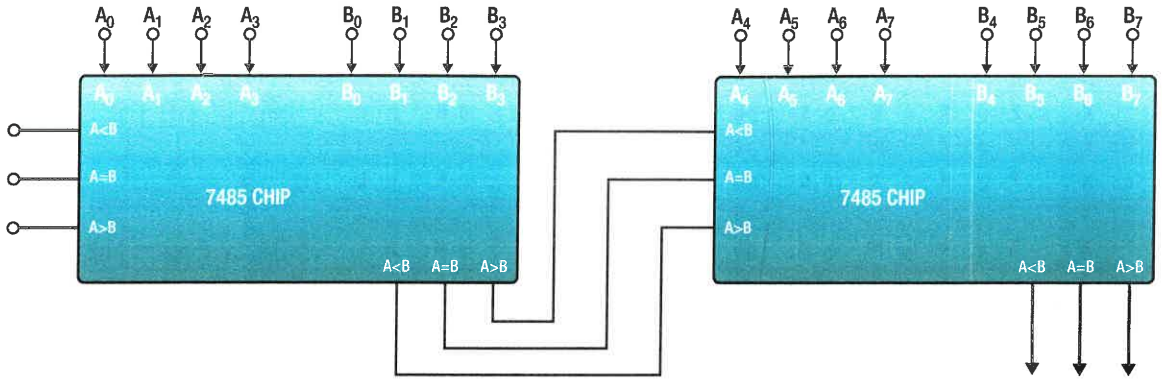


Figure 8-8. 7485 comparator cascading diagram.

To compare 32 versus 24, the Binary Coded Decimal (BCD) of 3 (0011) is applied to terminals A_0 through A_3 with A_3 being the Most Significant Bit (MSB), which is 0, and A_0 being the Least Significant Bit (LSB), which is 1; the BCD of 2 (0010) is applied to A_4 through A_7, with A_7 being the MSB, and A_4 being the LSB. Likewise, for the decimal 24, the BCD of 2 (0010) would be applied to B_0 through B_3 and the BCD of 4 (0100) would be applied to B_4 through B_7. In this example, the tens comparator (on the left) would output A>B to the units comparator (on the right), thereby passing the result directly through the units comparator since it is not needed to perform a comparison of units. However, if the BCD input to the A terminals is decimal 18 and the BCD input to the B terminals is decimal 14, the tens comparator would allow the units comparator to perform the comparison since the difference between the two decimals is in the units place, not in the tens place.

ENCODERS

The function of an encoder is to convert decimal numbers to binary numbers or binary-coded decimals. ***Figure 8-9*** illustrates the functional equivalent of an encoder that generates a 3-bit binary code corresponding to a switch position. In the example shown, switch position 4 results in a binary coded output of 4 = 1, 2 = 0, and 1 = 0, or binary 100, which corresponds to decimal number 4. Likewise, in ***Figure 8-10***, the compass needle pointing east provides a +5v input to D2 of the 74148 chip, an 8-line decimal to 3-line BCD encoder, which results in a binary code of 010 corresponding to an angular position of decimal number 2 or octal number 8.

In systems where two or more inputs may go HIGH (logic 1) simultaneously, a priority encoder is used to establish which input will be used. A priority encoder produces an output signal in accordance with a priority scheme based on the magnitude of the decimal numbers appearing at the input of the encoder. ***Figure 8-11*** is an illustration of the pin connections and truth table of the 74147, a 10-line decimal to 4-line BCD priority encoder. The 74147 chip is classified as an "active LOW" encoder since there are inverters present at the inputs

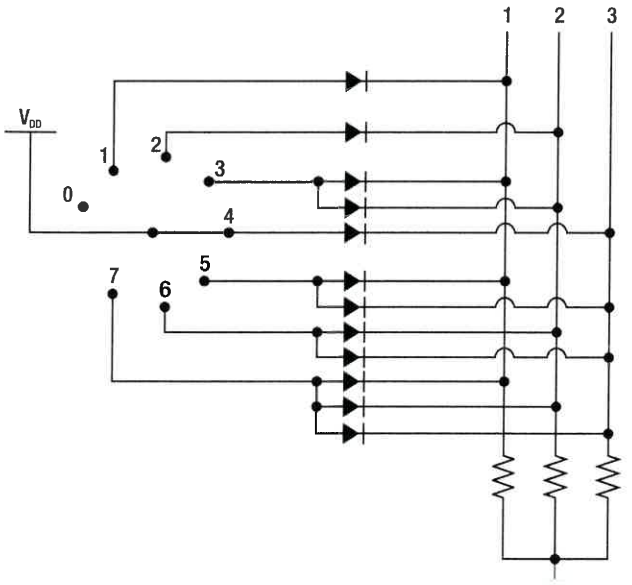


Figure 8-9. Simple digital encoder circuit.

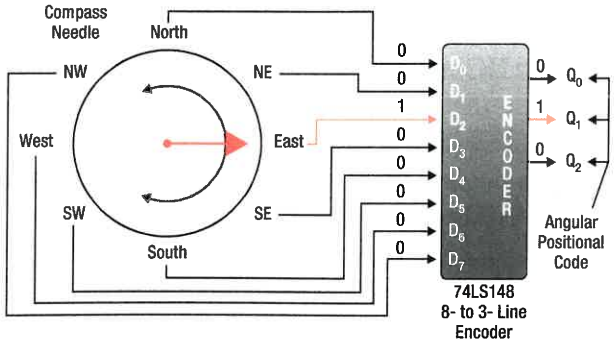


Figure 8-10. 74148 chip (8-line to 3-line encoder).

SN54/74LS147 FUNCTIONAL TABLE

1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	L	H	H	L	H	L
X	X	X	L	H	H	H	L	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH LOGIC LEVEL L = LOW LOGIC LEVEL X = IRRELEVANT

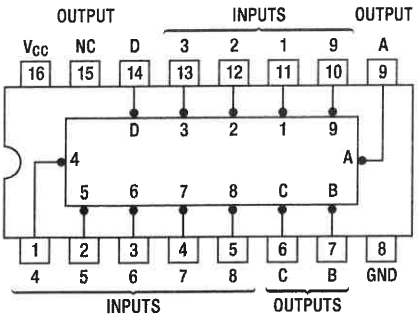
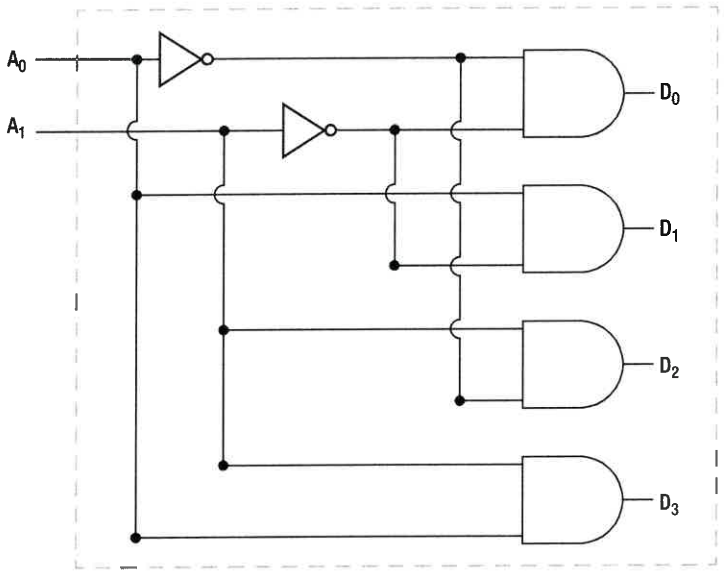


Figure 8-11. 74147 chip (10-line to 4-line priority encoder) with truth table.



A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Minterm Equations

$D_0 = \overline{A_1} \cdot \overline{A_0}$

$D_1 = \overline{A_1} \cdot A_0$

$D_2 = A_1 \cdot \overline{A_0}$

$D_3 = A_1 \cdot A_0$

Figure 8-12. 2-line to 4-line decoder.

and outputs such that these inputs and outputs become active at the LOW (logic 0) level. The outputs at A, B, C and D correspond to the highest-order LOW input with decimal 9 having the highest priority and decimal 1 having the lowest priority. All other inputs are irrelevant (as denoted by the "X" in the truth table). Note that the zero condition does not require any LOW inputs since zero is automatically encoded when all of the 9 inputs are set to HIGH.

DECODERS

Decoders perform the opposite function of encoders in that they convert binary numbers in to decimal numbers. For example, the 2-bit decoder, shown in ***Figure 8-12***, contains 2 inputs denoted by A_1 and A_0 (with A_1 being the most significant bit), and four outputs denoted by D_0, D_1, D_2, and D_3. The decoder enables one and only one of the four AND gates for each possible binary input. The two inverters provide the opposite logic inputs in the proper order to enable each gate based on the binary number input resulting in HIGH outputs from either D_0, D_1, D_2, or D_3 representing decimal numbers 0, 1, 2, or 3 respectively. For example, if the inputs are binary 00, then the output will be decimal 0; however, if the inputs are binary 11, then the output will be decimal 3.

Increasing the binary number input from 2 bits to 3 bits increases the number of outputs to 2_3 or 8 bits, resulting in a 3-Line to 8-Line decoder. ***Figure 8-13*** depicts the truth table, logic diagram, and pin-out of the 74138 chip, a 3-Line to 8-Line decoder with an enable line. The enable input performs no logical operation but is only responsible for making the decoder either active or inactive. As

10-LINE TO 4-LINE TRUTH TABLE

E	A_2	A_1	A_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	×	×	×	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
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1	1	1	1	1	0	0	0	0	0	0	0

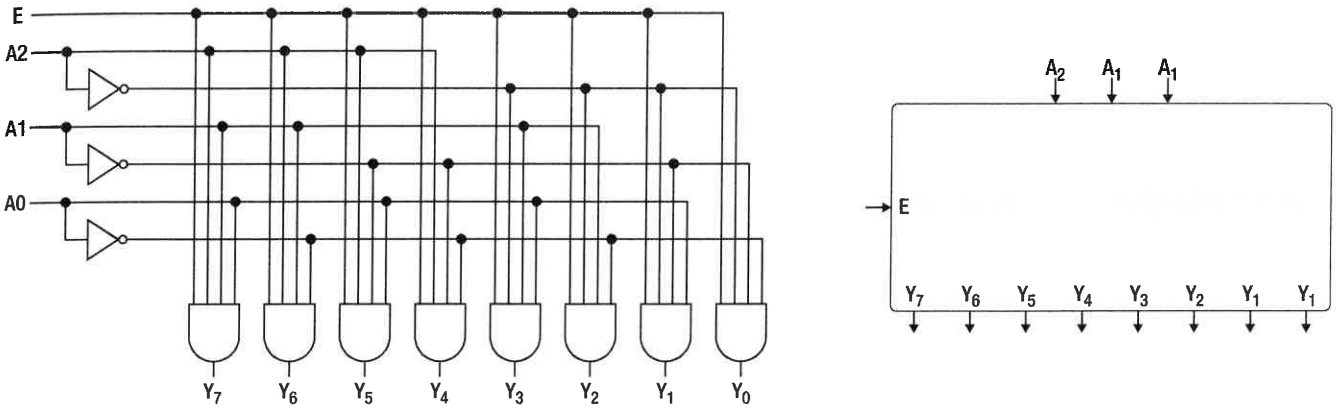


Figure 8-13. 74138 chip (3-line to 8-line decoder).

shown in the truth table, if the enable line is LOW, then all the outputs will be LOW regardless of the A_0, A_1 and A_2 input values (shown as "X" for don't care).

However, if the enable line is HIGH, then the decoder will perform its normal operation. The 74138 chip actually has three enable inputs, two of which are inverted, meaning the enable code must be binary 001 in order for the encoder to produce an output. In the example shown, the first two enable pins are assumed to be grounded (logic 0) so that only one enable line is used for making the decoder active or inactive.

Figure 8-14, illustrates a practical application of a decoder using a 7447 chip, a 4-line to 7-line decoder, to illuminate individual segments of a 7-segment liquid crystal display (LCD) based on the BCD input 0000 (0) through 1001 (9), presented to the decoder. Such displays are commonly found on aircraft communication, navigation and surveillance radio control panels.

Larger decoders can be built by using combinations of smaller ones. For example, an 8-line to 64-line decoder can be made by using four 4-line to 16-line decoders and one 2-line to 4-line decoder. Often, decoders and encoders are used together to decode binary data into decimals for a particular application and then encoded back for a different application. (***Figure 8-15***)

SCALE OF INTEGRATION

Integrated circuits are classified by their scale of integration, in other words, the number of transistors and other electronic components that they contain. Small-Scale Integration (SSI) circuits first appeared in the 1960's. They contained anywhere from 10 to 100 electronic components on a chip and were used to perform basic logic gate functions. (***Figure 8-16***)

Since the 1960's, there has been approximately a ten-fold increase per decade on the number of transistors on a chip. For example, in the early-1970's, Medium-Scale Integration (MSI) circuits first appeared having anywhere from 100 to 3 000 electronic components per chip. MSI circuits are used for adders, counters, registers, comparators, encoders, decoders, multiplexers, de-multiplexers, etc. (***Figure 8-17***)

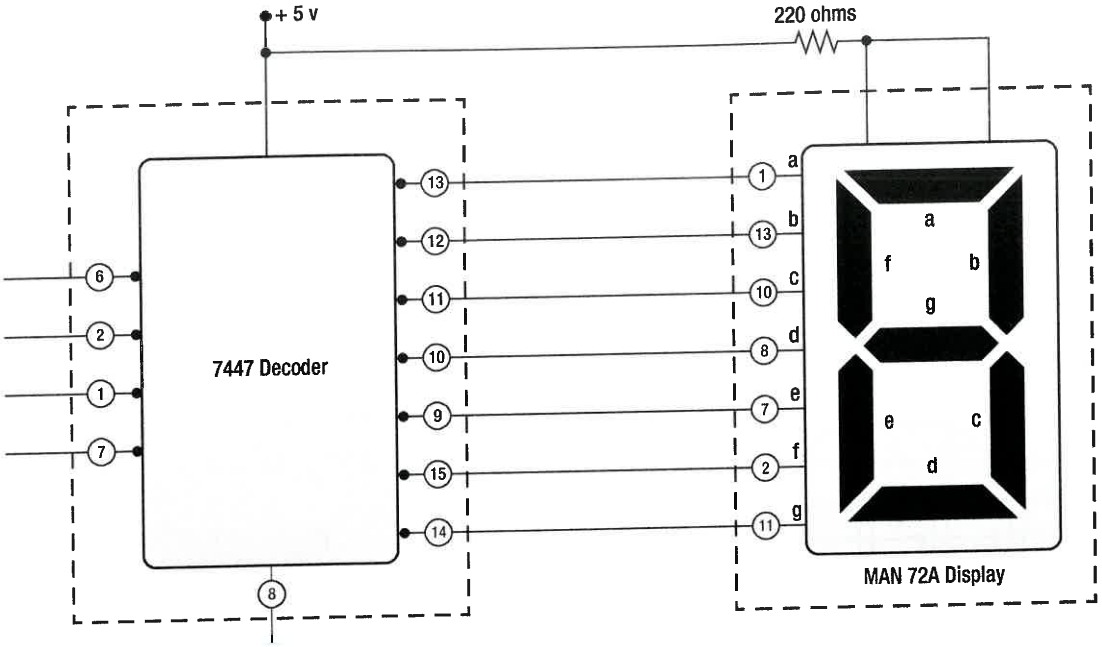


Figure 8-14. 7447 chip (4-line to 7-line decoder) with 7 AND/OR Gates to drive a 7 segment LED display.

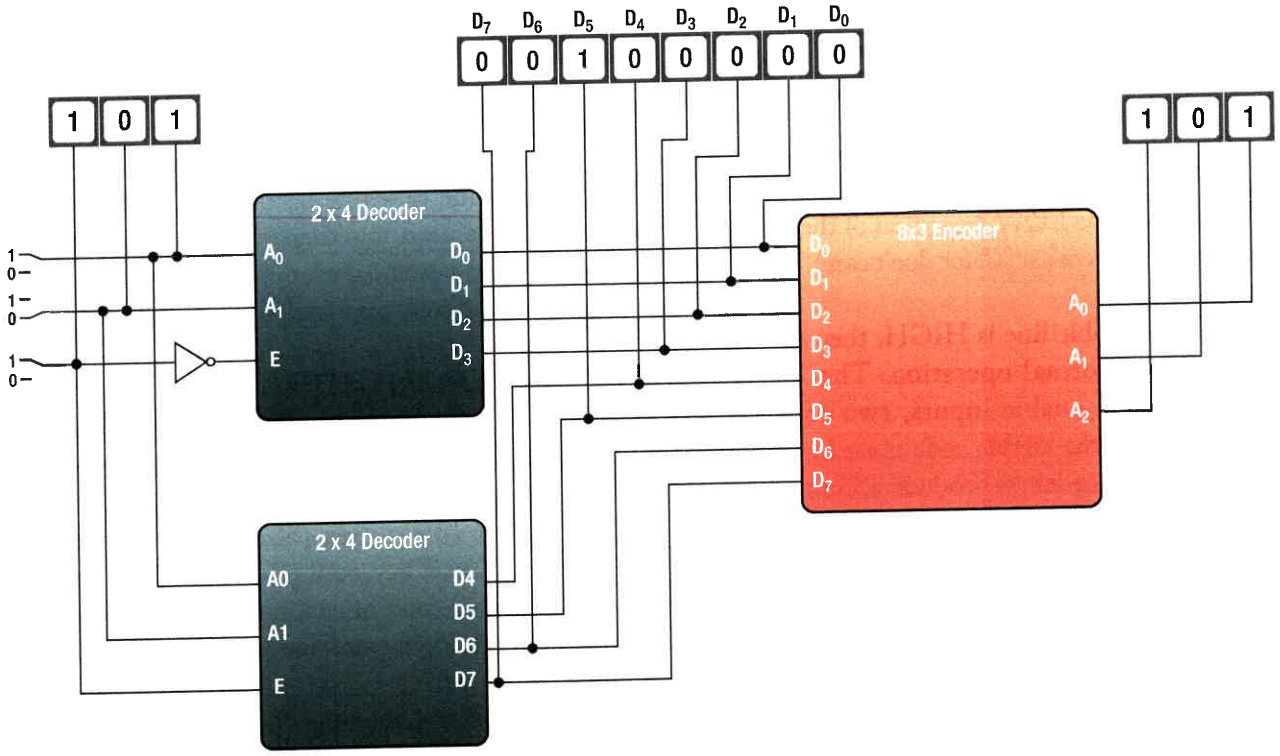
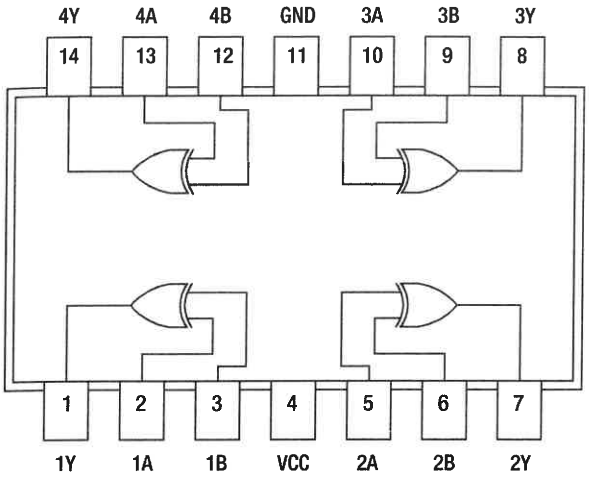


Figure 8-15. Decoder-encoder interconnect circuit.

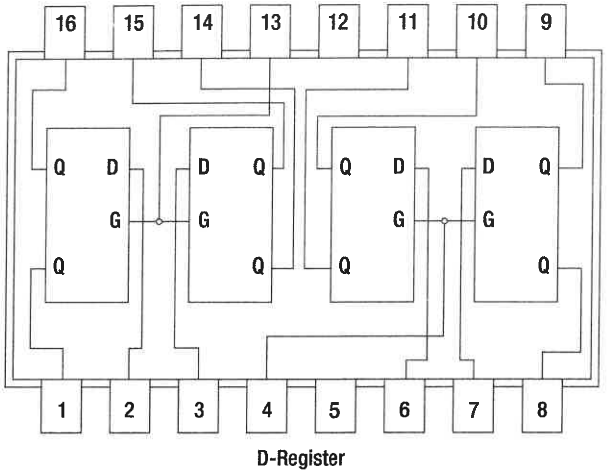
The first microprocessor, the 4-bit 4004 logic chip, appeared in 1971 in hand-held calculators. The 4004 chip contained 2 300 transistors running at a speed of 0.06 MIPS. (***Figure 8-18***) By the late 1970's, Large-Scale Integration (LSI) circuits with chips containing from 3 000 to 100 000 electronic components per chip were developed. These were used primarily for main memory modules and I/O controllers. In 1981, the first IBM Personal Computer appeared on the market with a 16-bit 8088 microprocessor chip, running at 0.75 MIPS and containing 29 000 transistors.



Quad exclusive-OR circuit

INPUT		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Figure 8-16. Small-scale integration schematic example.



D-Register

Figure 8-17. Medium-scale integration schematic example.

It's important to note that increasing the number of transistors on a chip increases the speed that the device can switch due to reduced gate delay times. However, the faster the chip operates, the more power it consumes, requiring heat-sinks to be installed over or under the IC package to reduce its operating temperature so that the component doesn't destroy itself.

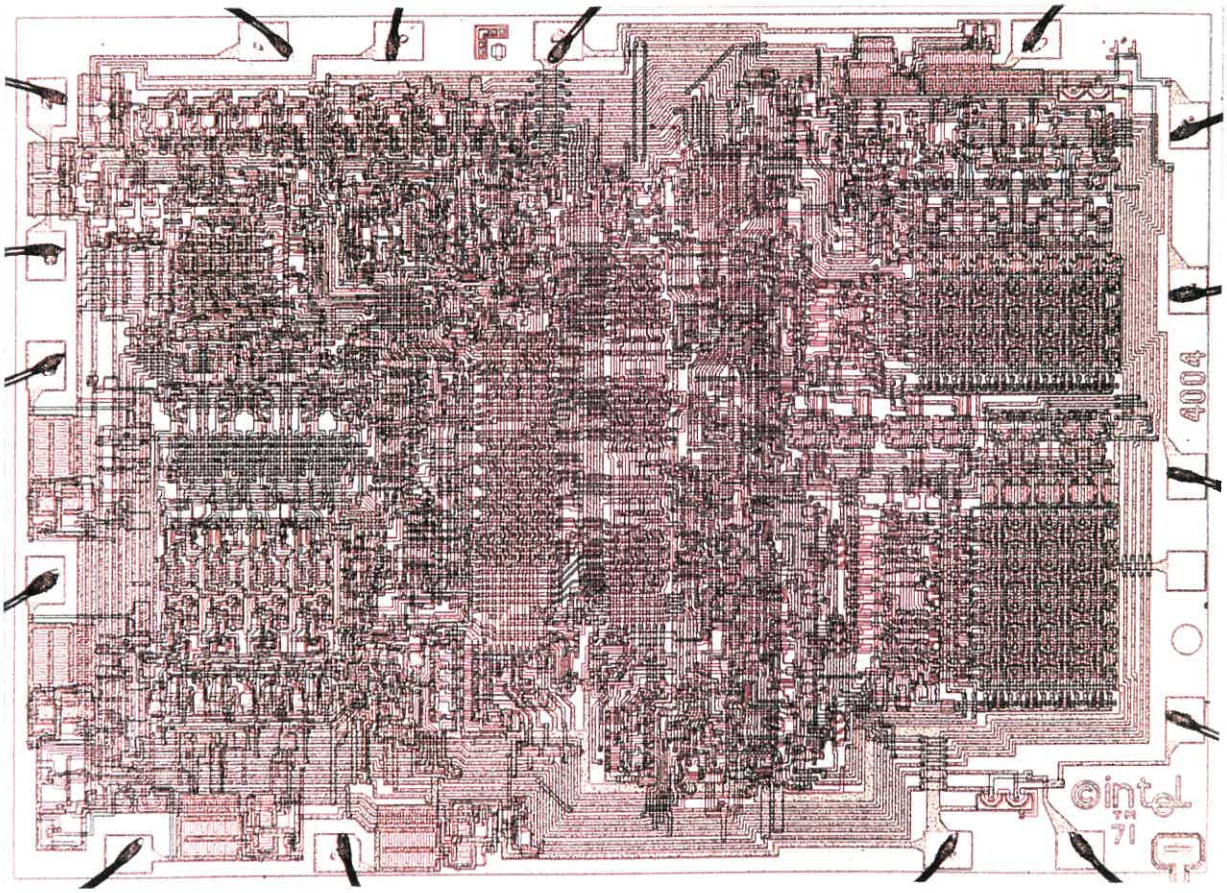


Figure 8-18. Intel 4004, the first microprocessor chip contained 2 300 transistors.

In the 1980's, Very-Large-Scale Integration (VLSI) circuits with 100 000 to 1 000 000 electronic components per chip became available allowing much faster processors with greater memory capacity which gave rise to a burgeoning software industry producing operating systems, such as Windows, and a multitude of application programs that were previously unavailable. Finally, Ultra-Large-Scale Integration (ULSI) circuits with more than one million electronic components per chip were developed. By 1993, the 32-bit Intel Pentium microprocessor chip appeared on the market containing 3.1 million transistors and running at speeds up to 100 MIPS.

By 2012, System-On-Chip integration became a reality with entire electronic systems being produced on a single chip containing 9 million transistors with the width of the conductor between the components on the chips measured in tens of a nanometer (one nanometer = one billionth of a meter). Moore's Law says that every 18 months, processing speed will double. As can be seen from the previous examples, this prediction has held true. However, chip level integration is quickly coming to point where smaller component feature sizes are approaching the limits of physics.

Question: 8-1
How are Integrated Circuit chips manufactured?

Question: 8-2
What are flip-flops and what purpose do they serve?

Question: 8-3
When using flip-flops, it is often desirable to establish the logic level outputs at a time other than when the signals are initially applied. How is this accomplished?

Question: 8-4
What is the advantage of a JK Flip-Flop over an RS Flip-Flop?

Question: 8-5
What is the purpose of a Comparator?

Question: 8-6
What is the difference between an Encoder and a Priority Encoder?

Question: 8-7
What function does the Decoder enable line perform?

Question: 8-8
What occurs as the number of transistors on a chip increases?

ANSWERS

Answer: 8-1
Chips are manufactured from a wafer of a thin substrate of semiconductor material, which is then processed in to thin round wafers. The electronic circuits are etched into the wafers using photo lithographic and chemical processing steps. The wafers are then polished, cleaned, and inspected. The individual chips are cut from the wafers and mounted in plastic or ceramic packages. Tiny wires are soldered from the chip to the connector pins.

Answer: 8-2
Flip-flops are bi-stable multi-vibrator circuits that form basic storage units of sequential logic used in shift registers and counters. They have the ability to maintain their state without further application of a signal allowing them to store a bit of data or one place of a larger binary number. Their ability to set one condition and reset or change to an alternate condition results in a latch, also known as a flip-flop.

Answer: 8-3
This is accomplished using a flip-flop circuit that is triggered by a clock input. The clock pulse acts as the control to allow the signals that appears at inputs of the S and R gates to pass to the cross-coupled flip-flop.

Answer: 8-4
The JK flip flop has the distinct advantage that they are no disallowed combinations as with the RS flip flops.

Answer: 8-5
Unlike a flip-flop that counts and stores binary numbers, the function of a comparator is to compare sets of binary numbers. Comparators are often used as parity checkers.

Answer: 8-6
The function of an encoder is to convert decimal numbers to binary numbers or binary-coded decimals. In systems where two or more inputs may simultaneously be HIGH, a priority encoder is used to establish which input will be used. A priority encoder produces an output signal in accordance with a priority scheme based on the magnitude of the decimal numbers appearing at the input of the encoder.

Answer: 8-7
The enable input performs no logical operation but is only responsible for making the decoder either active or inactive. If the enable line is LOW, then all the outputs will be LOW regardless of the input values. However, if the enable line is HIGH, then the decoder will perform its normal operation.

Answer: 8-8
Increasing the number of transistors on a chip increases the speed that the device can switch due to reduced gate delay times. However, the faster the chip operates the more power it consumes, requiring heat-sinks to be installed over or under the package to reduce its operating temperature so that the component doesn't destroy itself.

DIGITAL TECHNIQUES ELECTRONIC INSTRUMENT SYSTEMS

MULTIPLEXING

SUB-MODULE 09

PART-66 SYLLABUS LEVELS

CERTIFICATION CATEGORY → B2

Sub-Module 09

MULTIPLEXING

Knowledge Requirements

5.9 - Multiplexing

Operation, application and identification in logic diagrams of multiplexers and demultiplexers. 2

5.9 - MULTIPLEXING

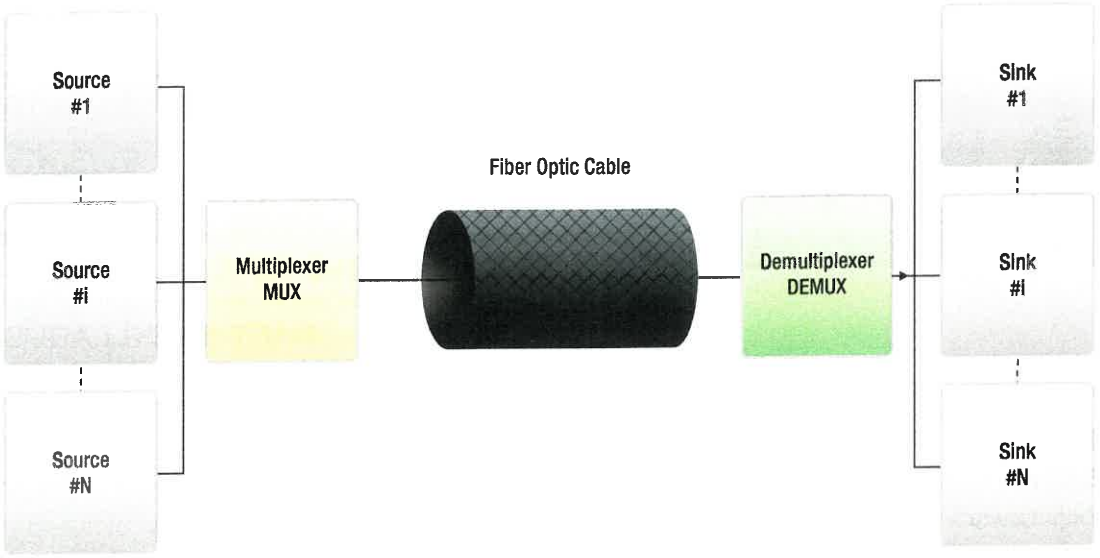


Figure 9-1. Multiplexing allows multiple signals to be transmitted through a single cable.

The previous Sub-Modules discussed IC logic circuits such as adders, flip-flops, comparators, encoders, and decoders. This *Sub-Module* will discuss another type of IC logic circuit, data multiplexers and demultiplexers, which are the components used to form serial data buses.

As previously stated in *Sub-Module 04*, multiplexing enables different forms of information to be sequentially transmitted through a single communication medium, whether it be a copper wire cable or a fiber optic cable. In addition, multiplexing eliminates the need to have many heavy wire bundles running through the aircraft since multiple signals can be distributed at different times through the same composite link. A multiplexer (MUX) is used to sample input data sequentially and then stagger the different data samples in time to form a composite digital pulse train. By knowing the clock time and address of the various signals, a demultiplexer (DEMUX) at the receiving end decodes and distributes the individual signals to the various data sinks. (***Figure 9-1***)

MULTIPLEXERS

Multiplexers, also called data selectors, are logic circuits with many input lines but only one output line. Multiplexers operate like very fast-acting, multiple position rotary switches (***Figure 9-2***) connecting multiple inputs lines, called channels, to a single output. As such, they associate one of many inputs to a single output, but only one at a time. Multiplexers are

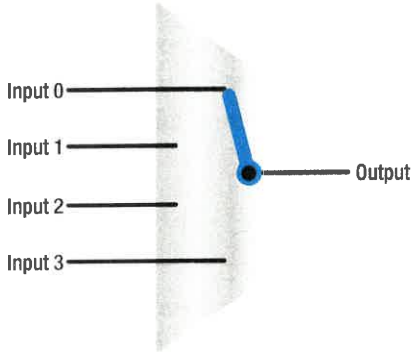


Figure 9-2. Multiplexer switches one of many inputs to just one output.

controlled by an additional set of inputs called select lines whereby the combination of binary codes to these select lines determine which data input is connected to the output.

Figure 9-3 is a representation of a 4-channel multiplexer circuit with 2 select lines (S_1 and S_0). As can be seen from the truth table, data will flow from one and only one data input (D_0, D_1, D_2 or D_3) at any one time depending on the binary code presented by the select inputs. For example, if S_1 = logic 1 and S_0 = logic 0, then the data stream from the D_2 input will pass directly to the output Y. The process of selecting 1 out of N input lines and transmitting the data to a single output line is called multiplexing. The purpose of the multiplexer is to select one and only one data source at a time to be transmitted to the demultiplexer for distribution.

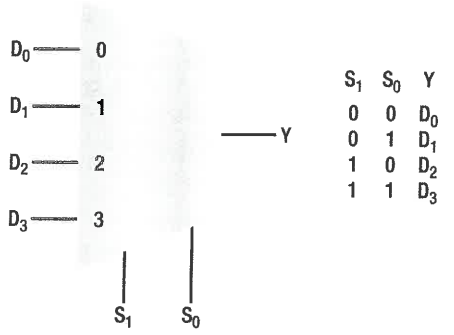


Figure 9-3. 4-Channel multiplexer symbol and truth table.

A 4-channel multiplexer, such as the 74153 chip, is constructed from 2 inverters, 4 AND gates and 1 OR gate, as shown in ***Figure 9-4***. The AND gates, which control the output, are selected by the binary number inputs to the select lines, S_0 and S_1. The outputs of each of the AND gates are ORed together to provide a common output at Y. For example, as shown in the truth table, if S_0 = 0 and S_1 =0, then data at the input of I_0 will pass through to the output Y, and data from inputs I_1, I_2, and I_3 will be prevented from passing through the multiplexer until such time that the select line codes change from other than binary code 00. The select codes will change automatically based on a clock timing signal (not shown) such that each input will have the opportunity to transmit its data at a pre-determined time duration.

The multiplexer and demultiplexer signals must be synchronized on the digital data bus with a timing signal so that the appropriate source signals are correctly distributed to the intended sink destinations. This is accomplished using a clock that activates the enable "strobe" on the multiplexer. For example, ***Figure 9-5*** is the pin-out and truth table for the 74151 chip, an 8-channel multiplexer consisting of 6 address buffers, 8 AND gates, one OR gate plus a strobe inverter and an output inverter. The enable input ($\overline{G}$) is inverted so if the strobe is 1, the output at Y is 0 and the inverted output at $\overline{W}$ is 1, regardless of the state of the select inputs C, B, and A. However, once the clock triggers the enable strobe input with a 0, the select lines allow the outputs shown in the truth table. For example, if $\overline{G}$ is enabled (logic 0) and C, B, and A are binary 011, then D_3 will output its digital data stream on output Y and $\overline{W}$ for as long as $\overline{G}$ remains 0.

INTERLEAVING

In order for the various data inputs from the multiplexer to be properly reconstructed by the demultiplexer, the signals must be interleaved. For example, to send three messages, ABC, DEF, and GHI, from multiplexer channels 1, 2, and 3, the first letter of each message will be serially transmitted at the first clock strobe, followed by the second letter at the second strobe, and the third letter at the third strobe. The multiplexer output will then consist of a data stream of ADGBEHCFI broken down into 3 data packets such that packet 1 consists of ADG, packet 2 consists of BEH, and packet 3 consists of CFI. These packets will be reconstructed by the

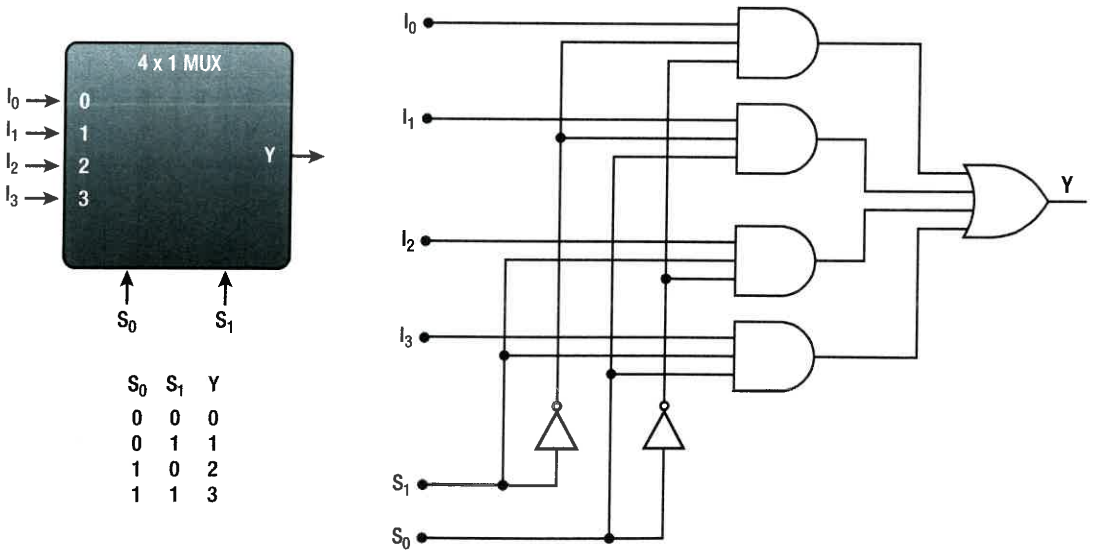
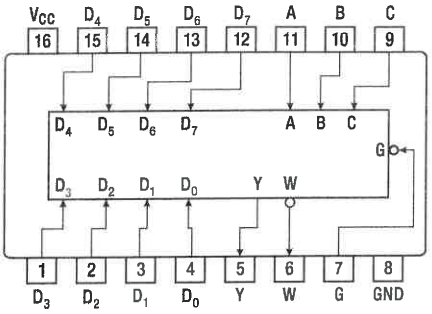


Figure 9-4. 74153 chip: 4-channel multiplexer logic diagram and truth table.



Inputs				Outputs	
Select			Strobe		
C	B	A	G	Y	$\overline{W}$
x	x	x	1	0	1
0	0	0	0	D_0	$\overline{D_0}$
0	0	1	0	D_1	$\overline{D_1}$
0	1	0	0	D_2	$\overline{D_2}$
0	1	1	0	D_3	$\overline{D_3}$
1	0	0	0	D_4	$\overline{D_4}$
1	0	1	0	D_5	$\overline{D_5}$
1	1	0	0	D_6	$\overline{D_6}$
1	1	1	0	D_7	$\overline{D_7}$

Figure 9-5. 74151 Chip: 8-Channel Multiplexer pin-out and truth table.

demultiplexer based on timing signals (strobes) that are synchronized with the multiplexer's timing signals. This method of signal interleaving is called Time-Division Multiplexing (TDM) because it divides the time during which each message is transmitted into time intervals. (***Figure 9-6***)

Besides TDM, other multiplexing methods used include Frequency-Division Multiplexing (FDM) and Wavelength-Division Multiplexing (WDM). Wavelength division multiplexing is used in some fiber optic data bus systems whereby the selection of the color of light passing through a single-mode fiber cable denotes the source and destination address.

DEMULTIPLEXERS

Demultiplexers perform the exact opposite function of multiplexers in that they associate one input with many outputs. Like multiplexers, they operate like very fast-acting multiple-position rotary switches; however, they connect one and only one channel (X) to multiple output lines (Y_0, Y_1, Y_2, Y_3, etc.), one at a time, as depicted in ***Figure 9-7***. Switching between data outputs is controlled by select lines (S_0, S_1), whereby the combination of binary codes to these select lines determine which data output is connected to the input at any given time.

A representation of a 4-channel demultiplexer logic diagram circuit (***Figure 9-8***) with 2 select lines (S_1 and S_0). As can be seen from the truth table, data will flow

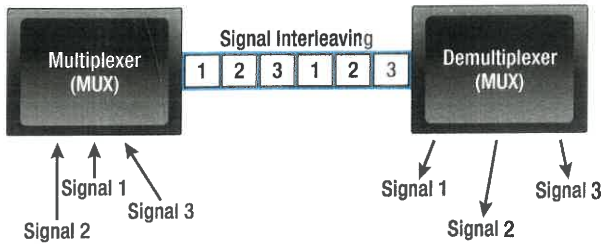


Figure 9-6. Time-division multiplexing concept.

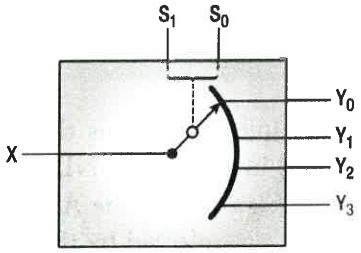
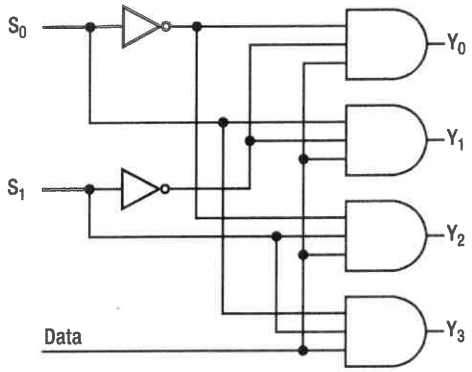


Figure 9-7. Demultiplexer switches one of many outputs from just one input.



S_1	S_0	X	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	0	0
0	1	1	0	0	1	0
1	0	0	0	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

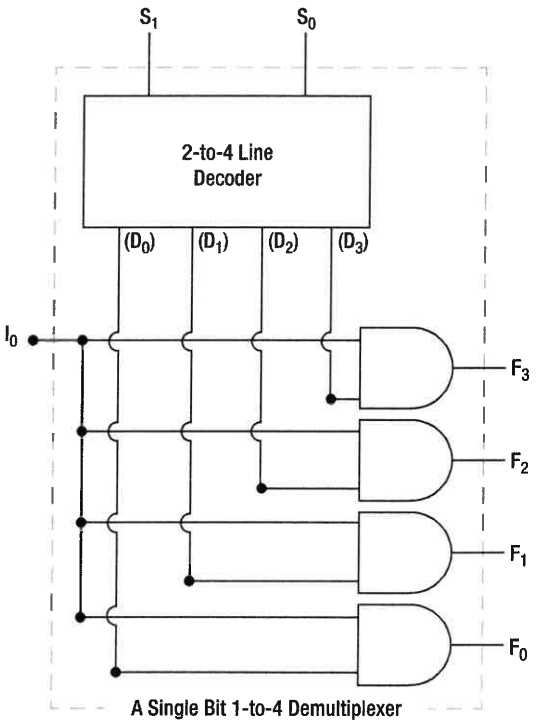
Figure 9-8. 4-Channel Demultiplexer logic diagram with truth table.

to one and only one data output (Y_0, Y_1, Y_2 or Y_3) at any one time depending on the binary code presented by the select inputs. For example, if $S_1 = 1$, $S_0 = 0$, and × (enable strobe) is 1 then the data stream will pass directly to output Y_2. Any time the enable strobe is set to 0, data will not be allowed to pass to any of the outputs. The process of receiving data on a single input line and selecting 1 out of N output lines for distribution

of the data is called demultiplexing. The purpose of the demultiplexer is to select one and only one data sink at a time to for data to be distributed. Again, the clock timing signals of the multiplexer and demultiplexer must be synchronized for proper data distribution.

Figure 9-9 is a variation of the previous demultiplexer circuit using a 2-line to 4-line decoder to control the 4 AND gates. The decoder enables one and only one of the AND gates to pass data from input I_0 to through either F_0, F_1, F_2, or F_3 outputs depending on the binary code provided by select lines S_0 and S_1, as shown in the truth table.

The 74138 chip, shown in ***Figure 9-10***, can be used as an 8-channel demultiplexer with its 8 NAND gates, 3 enable inputs (E_1, E_2, and E_3) inputs, and 3 buffered select lines (A_0, A_1, and A_2). Two of the enable inputs are inverted such that binary code 001 must be used to enable the demultiplexer. However, one of the enable lines can be used for data input and unused inverter inputs can be grounded. As shown in the ***Figure 9-11***, once the demultiplexer is enabled by the timing strobe, the binary codes from the select lines will determine which NAND gate is set active LOW to allow data to pass through one of the selected outputs (O_0 through O_7) for distribution.



Truth Table

S_1	S_0	I_0	F_3	F_2	F_1	F_0
0	0	0	0	0	0	0
		1	0	0	0	1
0	1	0	0	0	0	0
		1	0	0	1	0
1	0	0	0	0	0	0
		1	0	1	0	0
1	1	0	0	0	0	0
		1	1	0	0	0

Figure 9-9. 4-Channel Demultiplexer with 2-to-4 line decoder controller.

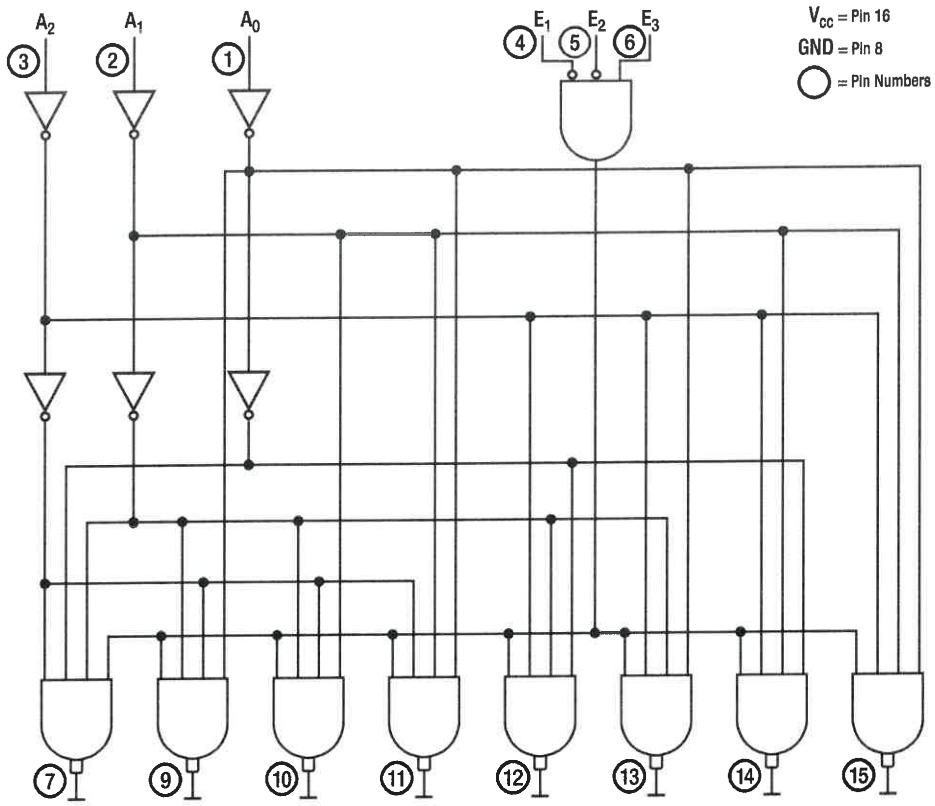
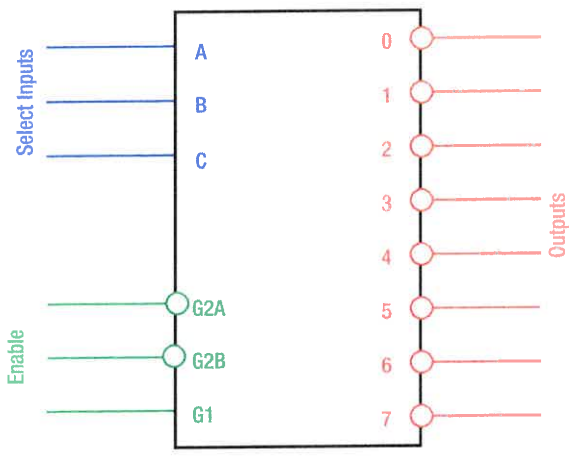


Figure 9-10. 74138 Chip: 8-Channel Demultiplexer logic diagram.



Inputs						Output							
Enable			Select										
G2A	G2B	G1	C	B	A	0	1	2	3	4	5	6	7
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

Figure 9-11. 74138 Chip: 8-Channel Demultiplexer truth table.

Question: 9-1
How does multiplexing allow multiple signals to be transmitted through a data bus?

Question: 9-2
What is the purpose of multiplexer select lines?

Question: 9-3
Why is it important that multiplexer and demultiplexer signals are synchronized?

Question: 9-4
Give an example how TDM signals are interleaved in order for the various data inputs from the multiplexer to be properly reconstructed by the demultiplexer.

Question: 9-5
Explain how Demultiplexers perform the exact opposite function of multiplexers.

ANSWERS

Answer: 9-1
Multiplexers are logic circuits with many input lines but only one output line. A multiplexer is used to sample input data sequentially and then stagger the different data samples in time to form a composite digital pulse train. By knowing the clock time and address of the various signals, a demultiplexer at the receiving end decodes and distributes the individual signals.

Answer: 9-2
The purpose of the multiplexer is to select one and only one data source at a time to be transmitted to the demultiplexer for distribution. Therefore, multiplexers are controlled by an additional set of inputs called select lines whereby the combination of binary codes to these select lines determine which data input is connected to the output.

Answer: 9-3
The multiplexer and demultiplexer signals must be synchronized on the digital data bus with a timing signal so that the appropriate source signals are correctly distributed to the intended sink destinations. This is accomplished using a clock that activates the enable "strobe" on the multiplexer.

Answer: 9-4
To send three messages, ABC, DEF, and GHI, from multiplexer channels 1, 2, and 3, the first letter of each message will be serially transmitted at the first clock strobe, followed by the second letter at the second strobe, and the third letter at the third strobe. The multiplexer output will then consist of a data stream of ADGBEHCFI broken down into 3 data packets such that packet 1 consists of ADG, packet 2 consists of BEH, and packet 3 consists of CFI. These packets will be reconstructed by the demultiplexer based on timing signals (strobes) that are synchronized with the multiplexer's timing signals.

Answer: 9-5
Multiplexers associate many inputs with one output while demultiplexers associate one input with many outputs. Like multiplexers, they operate like very fast-acting multiple-position rotary switches; however, they connect one and only one channel to multiple output lines one at a time.

DIGITAL TECHNIQUES ELECTRONIC INSTRUMENT SYSTEMS

FIBER OPTICS

SUB-MODULE 10

PART-66 SYLLABUS LEVELS

CERTIFICATION CATEGORY → B2

Sub-Module 10

FIBER OPTICS

Knowledge Requirements

5.10 - Fiber Optics

Advantages and disadvantages of fiber optic data transmission over electrical wire propagation;	2
Fiber optic data bus;	
Fiber optic related terms;	
Terminations;	
Couplers, control terminals, remote terminals;	
Application of fiber optics in aircraft systems.	

5.10 - FIBER OPTICS

Figure 10-1. Coaxial cable typically used for data rates of 2Mbps to 50Mbps.

Sub-Module 04 discussed various digital data buses, such as MIL-STD-1553B and ARINC 629, which use shielded twisted-pair copper wires for transmitting information at data rates of one to two millions bits per second (Mbps). From 2 Mbps to 50 Mbps, coaxial cable is the preferred transmission medium. Coaxial cable, also known as coax, consists of a center wire conductor surrounded by a semi-rigid insulator. Surrounding the wire and the insulator material is a conductive, braided cover that runs the length of the cable. Finally, a waterproof covering is set around the braided shield to protect the entire assembly from the elements. The braided cover in the coax shields the inner conductor from any external electro-magnetic fields. It also prevents the fields generated by the internal conductor from radiating. (***Figure 10-1***)

Aircraft networks, such as AFDX and Firewire, with data rates running as high as 1000 Mbps, or one gigabit per second (Gbps), require the use of fiber optic cables to reliably transmit large bandwidths of information. As shown in ***Figure 10-2***, a fiber optic cable consists of the core, which is a thin glass or plastic center where the light travels, surrounded by an outer optical material, called a cladding, which reflects the light back into the core, and a black polyurethane outer jacket over the cladding to protect the cable from damage and moisture. If the fibers in the core are made from glass there will also be a plastic coating applied to the cladding, called a buffer jacket, to provide additional protection. Materials made from fiberglass or Kevlar add mechanical strength to the cable.

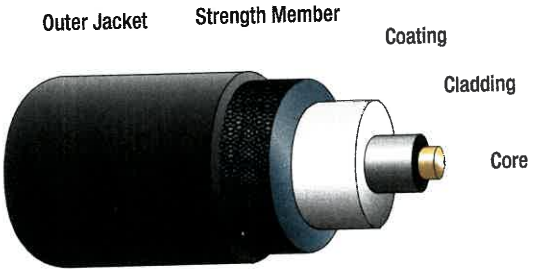


Figure 10-2. Fiber optic cable used for data rates as high as 1Gbps.

ADVANTAGES AND DISADVANTAGES

Besides having a high data-rate capability and a wide bandwidth to carry more information, optical buses exhibit extremely low loss and low crosstalk since there is no line capacitance or mutual coupling. The reason why optical cables exhibit such low loss is because there is very little attenuation, or reduction in signal strength, over long distances as compared to copper wire. Cables made from silica glass fibers have the lowest attenuation, and as such, are widely used in the telecommunications industry for large bandwidths and long distances. Plastic fibers are less expensive, extremely rugged and have a tight bend radius, but exhibit a higher loss.

Tensile strength is the ability of a fiber or wire to be stretched without breaking. Copper wire must have twice the diameter to have the same tensile strength as a glass fiber. When installing fiber cable, care must be taken not to exceed its recommended bend radius since a sharp bend will decrease the tensile strength and may snap the glass. Sharp bends will also increase attenuation since the bends change the angle of incidence and reflection of the light. The chief advantage of optical cables are that they are immune from electro-magnetic interference (EMI). Copper conductors will act like antennas, either transmitting or receiving energy. Copper wires connecting avionics equipment can be one of the main sources of EMI, which can cause errors to occur during digital data transmissions. Optical cables can also withstand nuclear radiation in that the fibers will not short out if their jackets melt.

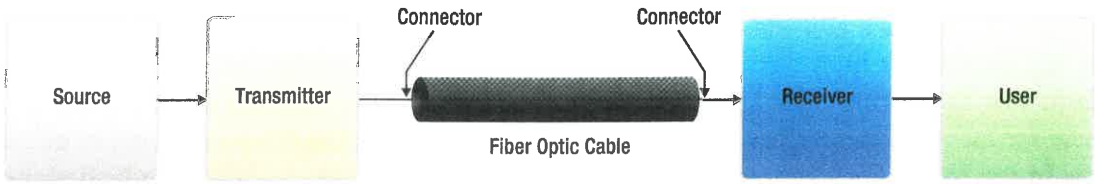


Figure 10-3. Basic fiber optic link.

All though optical cables are lighter than copper cables, they are generally more expensive and require the use of optical transmitters and receivers. In addition, fibers are more difficult and expensive to splice than copper wires. However, the advantages of fiber optic networks far outweigh the disadvantages of electrical data buses for the reasons stated above.

FIBER OPTIC DATA BUS

A fiber optic data bus operates basically the same as an electrical data bus except that the fiber carries light instead of electricity. As shown in ***Figure 10-3***, a basic fiber optic link connects two electrical circuits from the data source to the data sink (user) using a light source, transmitter, fiber optic cable, and receiver to provide information to the user. The light source can be either a Light Emitting Diode (LED) or a laser diode. The laser diode has a higher output power and faster speed than an LED, but it is more expensive. The transmitter converts electrical signals into light pulses and sends the pulses over the fiber optic cable to the receiver.

The purpose of the receiver is to rebuild the signals back to their original state as they were presented to the transmitter. The two basic parts of the receiver are the photocell, also called a photodiode detector, which converts the light back into an electrical signal; and the output circuit, which amplifies and reshapes the signal back into its original digital data stream. Clock information is either contained in the transmitted signal or the receiver may provide its own timing information to decode and reshape the digital pulse train. The following paragraphs will compare and contrast various fiber optic transmitter and receiver circuits.

TRANSMITTERS

To reiterate, fiber optic transmitters consist of a driver and a source. The input to the driver is the binary code used to turn the current on and off to the light source, whether it be an LED or a laser diode. The op-amp driver accepts either TTL or CMOS logic levels and provides the output current to drive the source. For example, the drive circuit would convert 0.5v (bit "0") and 5v (bit "1") of TTL binary logic into 0 ma and 50 ma respectively to modulate the light source off and on. A modulation code is used as a method of encoding digital data such that turning the source on and off forms Pulse-Coded Modulation (PCM) waveforms that correspond to binary number equivalents, as shown in ***Figure 10-4***.

Each bit of data must occur within its bit period, which is defined by the transmitter clock. The clock provides a steady string of pulses for basic system timing. Some codes are self-clocking, meaning that the clock information is contained within the modulation code. However, a receiver may provide its own timing, and not rely on clock signals from the transmitter, if it designed to receive non-self-clocking code.

DECIMAL NUMBER	BINARY EQUIVALENT				PULSE – CODE WAVE FORMS
	2^3	2^2	2^1	2^0	2^3 2^2 2^1 2^0
0	0	0	0	0	
1	0	0	0	1	
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	

Figure 10-4. Binary number to pulse-coded modulation translation table.

NRZ (non-return-to-zero) is a non-self-clocking code whereby the signal remains high during a string of 1s and remains low for a sting of 0s. (***Figure 10-5***) However, there are many different types of modulation codes that are in use today. For example, MIL-STD-1553B uses what is called Manchester Code, whereby there is a transition in the middle of each bit period. Manchester, which is a self-clocking code, is generated by placing an Exclusive OR gate between the clock pulse and the data pulse. As such, for a binary 1, the first half of the period is high, and the second half is low. For a binary 0, the first half is low and the second half is high. As a result, Manchester code has two symbols per bit, instead of one as in NRZ code. Therefore, to transmit a 1 Mbps data stream requires a bandwidth of 2 MBaud. Baud rate is the number of symbols or pulses per second.

LIGHT-EMITTING DIODES

LEDs operate on the principle of electroluminescence, which is a term used to describe a phenomenon whereby light emission is caused by the application of an electric current. Light contains electromagnetic energy that is carried by photons. The amount of energy depends on the frequency of light of the photon. In a forward biased diode, electrons cross the junction and fall into holes. As the electrons fall into the valence band, they radiate energy. In a rectifier diode, this energy is dissipated as heat. However, in a LED, the energy is dissipated as light. By using elements, such as gallium, arsenic, and phosphorous, an LED can be designed to radiate colors, such as red, green, yellow, blue and infrared light. ***Figure 10-6*** illustrates the anatomy of a single LED, the symbol of an LED, and a graphic depiction of the LED process. Note that when the diode is reversed biased, no light is given off. However, when the diode is forward biased, the energy given off is visible in the color characteristic for the material being used.

By modulating the bias of the LED, light pulses are formed to be sent over a fiber optic cable to a photodiode receiver. Different color LEDs can be employed in the transmitter to signify which receiver the signal is intended. This is known as Wavelength-Division Multiplexing (WDM). Light that is emitted by a semiconductor can be absorbed by the same semiconductor material in the receiver. WDM is used in some fiber optic data bus systems whereby the selection of the color of light passing through a fiber cable denotes the source and destination address

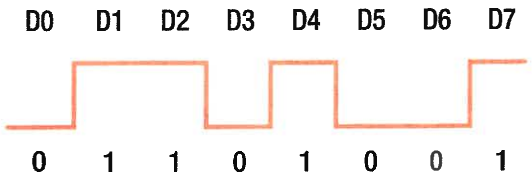


Figure 10-5. NRZ code.

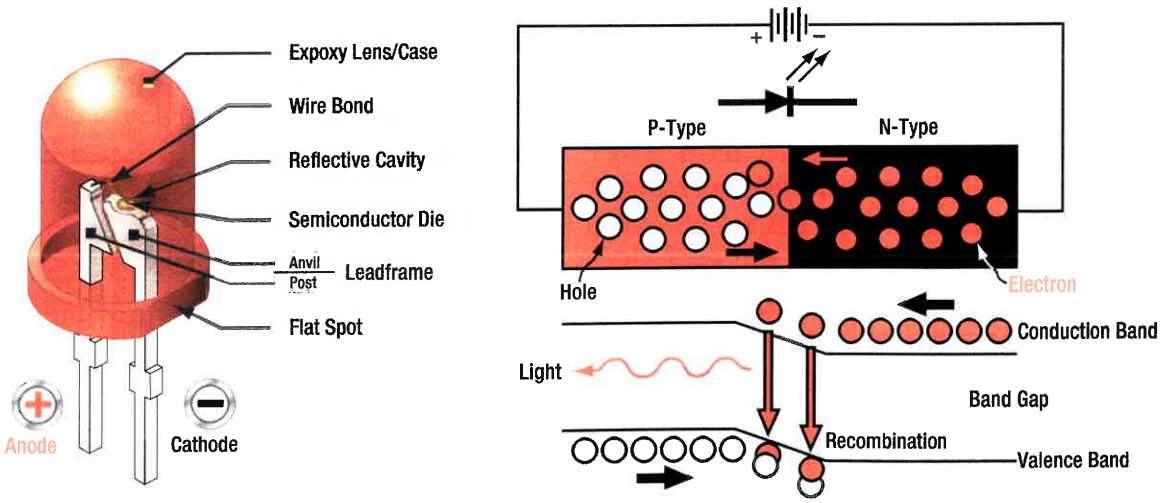


Figure 10-6. An LED producing light by electrons dropping into holes and giving off energy.

LASER DIODES

Laser is an acronym standing for Light Amplification by Simulated Emission of Radiation. The main difference between an LED and a laser diode (***Figure 10-7***) is that the laser diode has an optical cavity required to produce a laser beam. In general, laser diodes have higher modulation bandwidth, greater optical output power, and higher coupling efficiency to the fiber cable, and therefore, are widely used for high-speed digital applications. The reason why a laser diode has a higher coupling efficiency is due to its narrow spatial beam width. The amount of bias current applied to the laser diode controls the gain, and thus the light intensity. Photodiodes are often installed on the rear face of the cavity to monitor the light output to adjust the drive current to maintain a constant optical power level.

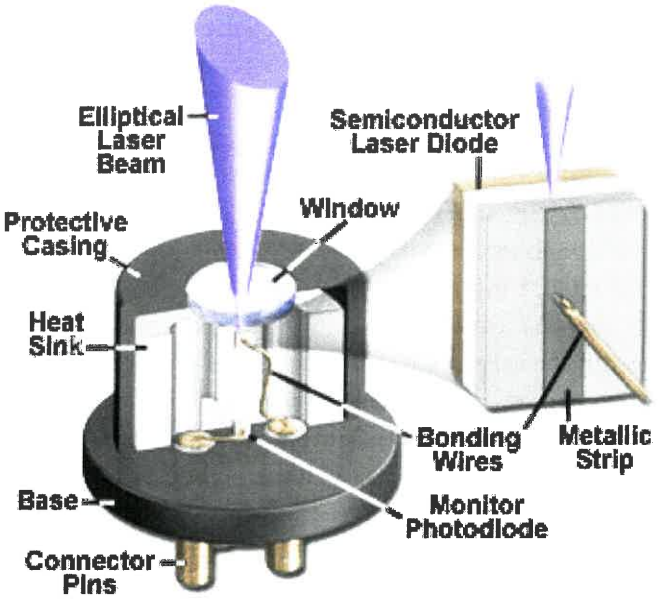


Figure 10-7. Anatomy of a laser diode.

As shown in ***Figure 10-8***, the semiconductor material used for a laser diode consists of an alloy of aluminum (Al) and gallium arsenide (GaN). Lasing is achieved through optical resonance whereby photons are generated due to a high current being applied across the semiconductor material. At low drive currents, the laser diode acts much like an LED in that it emits light spontaneously resulting in photon emission with random phase and direction. However, as the drive current increases, stimulated emission occurs, whereby electrons are injected into the laser diode and combine with holes forming photons. If one of these photons comes in contact with an electron, the electron immediately recombines and gives off another photon.

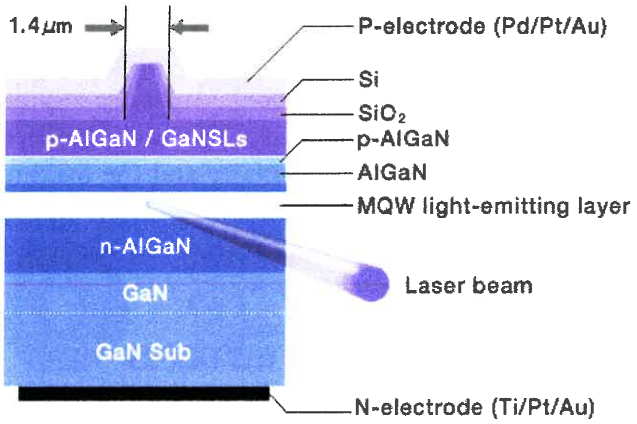


Figure 10-8. AlGaN semiconductor material is used to produce a laser beam.

The photon that has been created is a duplicate of the first proton in that it has the same wavelength, phase and direction of travel. These photons interact with more incoming electrons, helping to produce more photons, and so on in a self-perpetuating process called optical resonance. The emitted photons will resonate in the optical cavity, which is lined with reflective material, and will travel in the same direction with the same frequency and phase emitting an amplified beam of light from the open end of the cavity.

Fiber optic sources, such as high-radiance LEDs and lasers, emit intense infrared light invisible to the human eye. Such radiation can cause permanent damage to the retina of the eye and produce blindness. Never look directly into a source or into a fiber energized by a source!

RECEIVERS

A fiber optic receiver consists of a detector, amplifier, and output circuit. The output circuit is used to separate the clock signals from the data, reshape the data pulses back into their original format, and provide gain control to maintain constant output levels once the signal from the photo-diode detector is amplified. As shown in ***Figure 10-9***, light striking the photodiode causes current to flow in the circuit whereas the diode would have otherwise blocked it. The result is that the data pulse is allowed to pass through the receiver to be amplified and filtered.

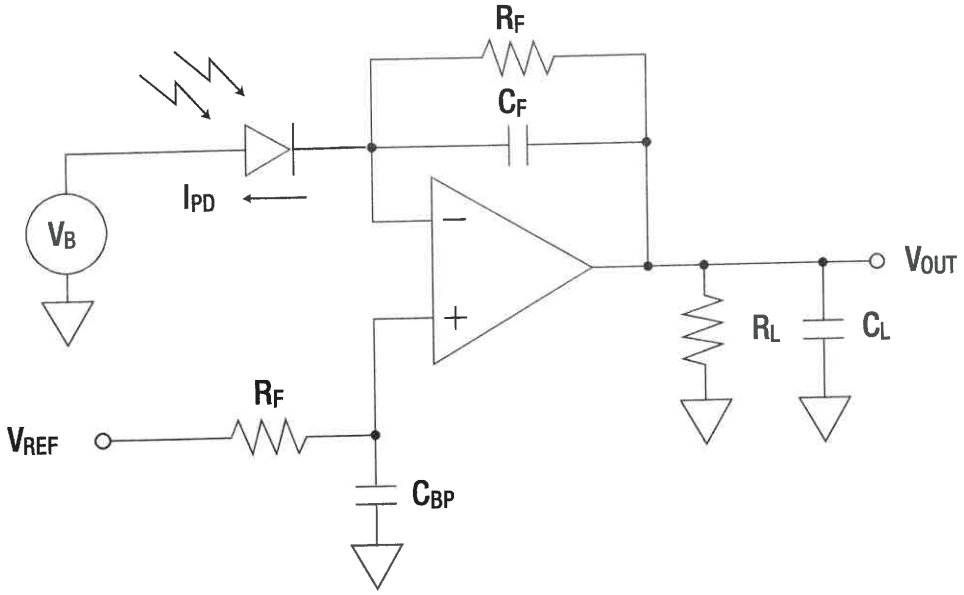


Figure 10-9. Fiber optic receiver with detector, Op-amp, and output circuit.

Receivers are classified based on their sensitivity and dynamic range. Sensitivity specifies the weakest optical signal that can be detected while rejecting noise. Dynamic range is the difference between the minimum and the maximum power levels. The minimum level is determined by receiver sensitivity and the maximum level is determined by the gain setting on the amplifier. Excessive power levels can saturate the receiver and distort the output signal.

PHOTO-DIODE DETECTORS

Light contains electromagnetic energy that is carried by photons. The amount of energy depends on the frequency of light of the photon. This energy can be very useful in the operation of fiber optic data buses since all semiconductors are affected by light energy. When a photon strikes a semiconductor atom, it raises the energy level above what is needed to hold its electrons in orbit. The extra energy frees an electron enabling it to flow as current. The vacated position of the electron becomes a hole. In photodiodes, this occurs in the depletion area of the reversed biased PN (positive-negative) junction turning on the device and allowing current to flow. (***Figure 10-10***)

Thermal energy produces minority carriers in a diode. The higher the temperature, the greater the current in a reverse current diode. Light energy can also produce minority carriers. By using a small window to expose the PN junction, a photodiode can be built. When light fall upon the junction of a reverse-biased photodiode, electrons-hole pairs are created inside the depletion layer. The stronger the light, the greater the number of light-produced carriers, which in turn causes a greater magnitude of reverse-current. Because of this characteristic, photodiodes are used in light detecting circuits, such as fiber optic data bus receivers.

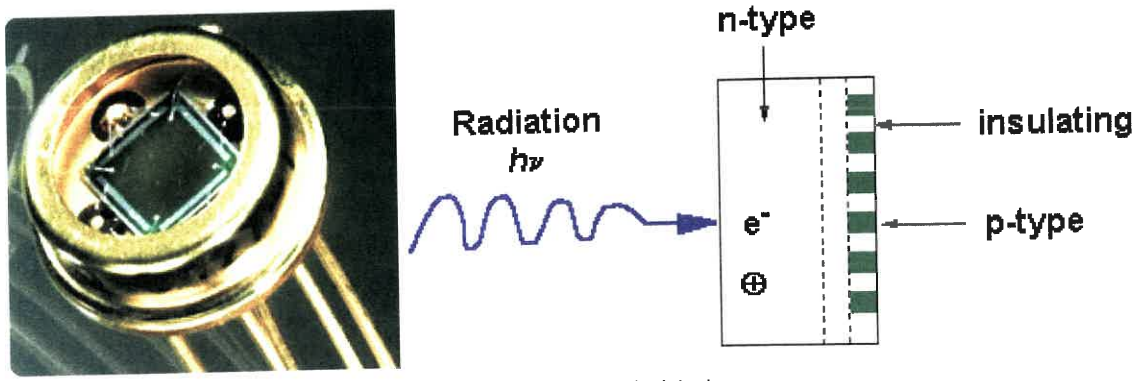


Figure 10-10. Photodiode detector.

RELATED TERMS

There are two types of fiber-optic cable that are available, single mode and multimode. As shown in ***Figure 10-11***, many beams of light travel through the multimode cable bouncing off of the cable walls. Attenuation is caused by the scattering and absorption of light as it travels down the fiber core. Light is reflected off the cladding, which acts like a mirror so that light can bend along its length. Scattering re-directs light out of the core to the cladding and absorption occurs when the light is not reflected back into the core, but instead is absorbed by the coating due to imperfections in the optical material. Single-mode fiber uses a single direct beam of light, thus allowing for greater distances and increased transfer speeds. Common types of fiber optic cable include the 62.5 micron core with 125 micron cladding multimode cable, 50 micron core with 125 micron cladding multimode cable, and the 9 micron core with 125 micron cladding single mode cable.

TERMINATIONS

Unlike copper wire, fiber optic cables can't be soldered or crimped to make a low resistance connection; however, it is equally important that fiber optic terminations couple light from one component to another with as little loss of optical power as possible. The key to low loss is precise alignment of the mated fiber cores so that nearly all the light is coupled from one fiber across the junction to the other fiber. Fibers must be checked for precise perpendicularity and end finish prior to termination. Mismatches can occur due to variations in tolerances between the diameter and concentricity of the core and cladding. In addition, connectors and splices can contribute to insertion losses due to variations in lateral displacement, end separation, angular misalignment and surface roughness.

The scribe-and-break method is commonly used to prepare fibers for termination. A cutting tool scribes a small nick across the cladding. The blade is then pulled across the stationary fiber. After scribing, pressure is increased on the cable by pulling it resulting in a clean break with a mirror-like finish. Once the fiber is prepared, splices can be made either by fusion or by using elastomeric inserts held within a glass sleeve. A fusion splice is accomplished by placing the two fibers on the V-grove of a splicing tool alignment block. The alignment is adjusted while viewing it though a microscope. Once aligned, an electric arc is applied. The localized heating softens the butted fiber ends and surface tension is applied during the fusion process. The finished splice is then encased in epoxy and heat-shrink tubing for protection.

Aircraft applications commonly use SMA (sub-miniature version A) fiber optic connectors due to their ruggedness. An SMA connector consists of a metal body assembly with a precision hole in the tip. (***Figure 10-12***) A stripped fiber, held within the alignment ferrule, is inserted into the body assembly and secured with epoxy. Strength members in the cable are then crimped between the body assembly and the eyelet to provide rigidity. The excess fiber is removed and then polished to the desired length and optical finish. The connector mates in a sleeve bushing with a screw-type coupling mechanism which provides a secure and aligned fit.

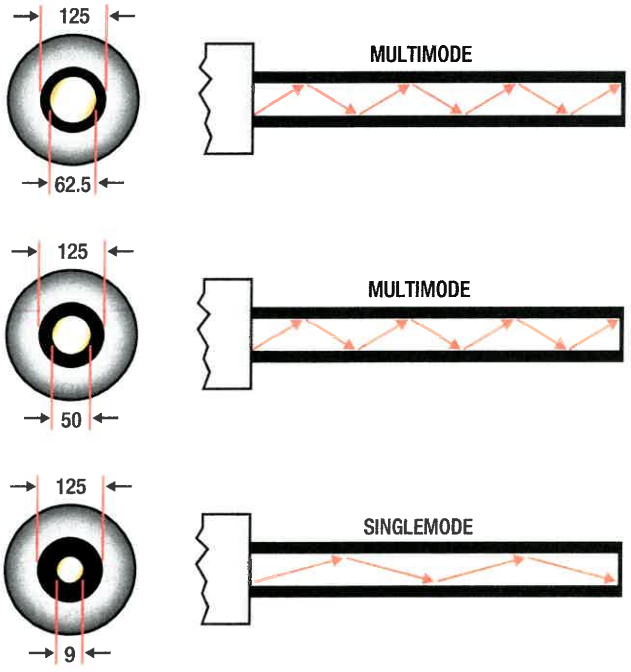


Figure 10-11. Multimode versus single mode fiber.

Figure 10-12. Standard SMA fiber optic cable connector.

COUPLERS AND TERMINALS

A coupler is a device that has multiple input or output ports for light to travel. ***Figure 10-13*** shows a four-port directional coupler. Such a device is fabricated by fusing together two single mode fibers so that their cores come close together, allowing light to leak from one core to the other. Light entering port 1 will be split and will exit ports 3 and 4. Ideally, no light will appear at port 2. Likewise, light entering port 2 should only exit ports 3 and 4. Losses will naturally occur within the coupler due to scattering, absorption, reflections and cable misalignment. Another type of coupler is the tee coupler, shaped as a "T", and used in the MIL-STD-1773 fiber optic data bus equivalent of MIL-STD-1553B.

A tee coupler at each remote terminal splits off a portion of the light from the data bus and carries it to the fiber optic transceiver in each terminal. The disadvantage of the tee coupler is that the optical power loss increases proportionally to the number of terminal nodes on the bus.

A star coupler, as shown in ***Figure 10-14***, has multiple ports to distribute the optical power point-to-point to multiple terminals. Unlike, the tee coupler, the insertion loss does not increase directly with the number of terminals; and therefore, it is well suited for connecting a large number of terminals to the fiber optic network. Directional couplers, tee couplers, and star couplers are called passive couplers because they allow the equal division of light between all the terminal nodes that are connected to them. However, an optical switch, such as used in the Avionics Full-Duplex Switched Network (AFDX) only allows light to be coupled from one fiber to another but not to both. As shown in ***Figure 10-15***, the AFDX optical switch permits one of two circuit paths to be chosen depending on the switch setting. This active switch uses a relay to physically move the fiber between two or more positions.

APPLICATIONS IN AIRCRAFT SYSTEMS

All though fiber optic networks are beginning to appear in some modern flight and engine control systems, they are more prevalent in In-Flight Entertainment (IFE) systems due to their high bandwidth characteristics. (***Figure 10-16***) Currently in development is a Fourth Generation Cabin Distribution System standard, which locates an active fiber optic data switch below the floor

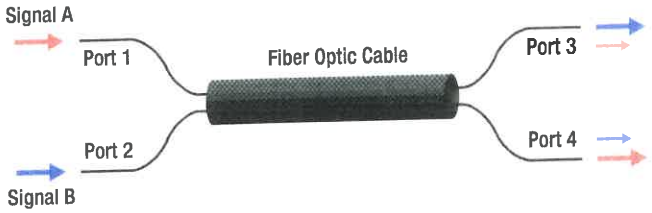


Figure 10-13. Four-port directional coupler.

Figure 10-14. A six-port star coupler.

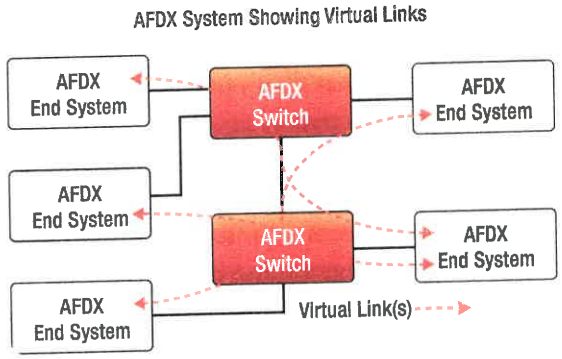


Figure 10-15. AFDX fiber optic network with active switches.

panels with fiber optic cabling routed to each of the passenger seats. Cabin systems are covered in much more detail in *Sub-Module 15*.

A fiber network failure may be observed as an increase in the bit error rate or a total failure in data transmission, which could be the result of a broken fiber, a source with no optical output, or circuit failure where there is a loss of modulation. No optical output could be caused by a laser that no longer reaches its threshold where stimulated emission occurs. It is important to note that fiber optic cable breakages do not cause intermittent failures, unlike copper wire.

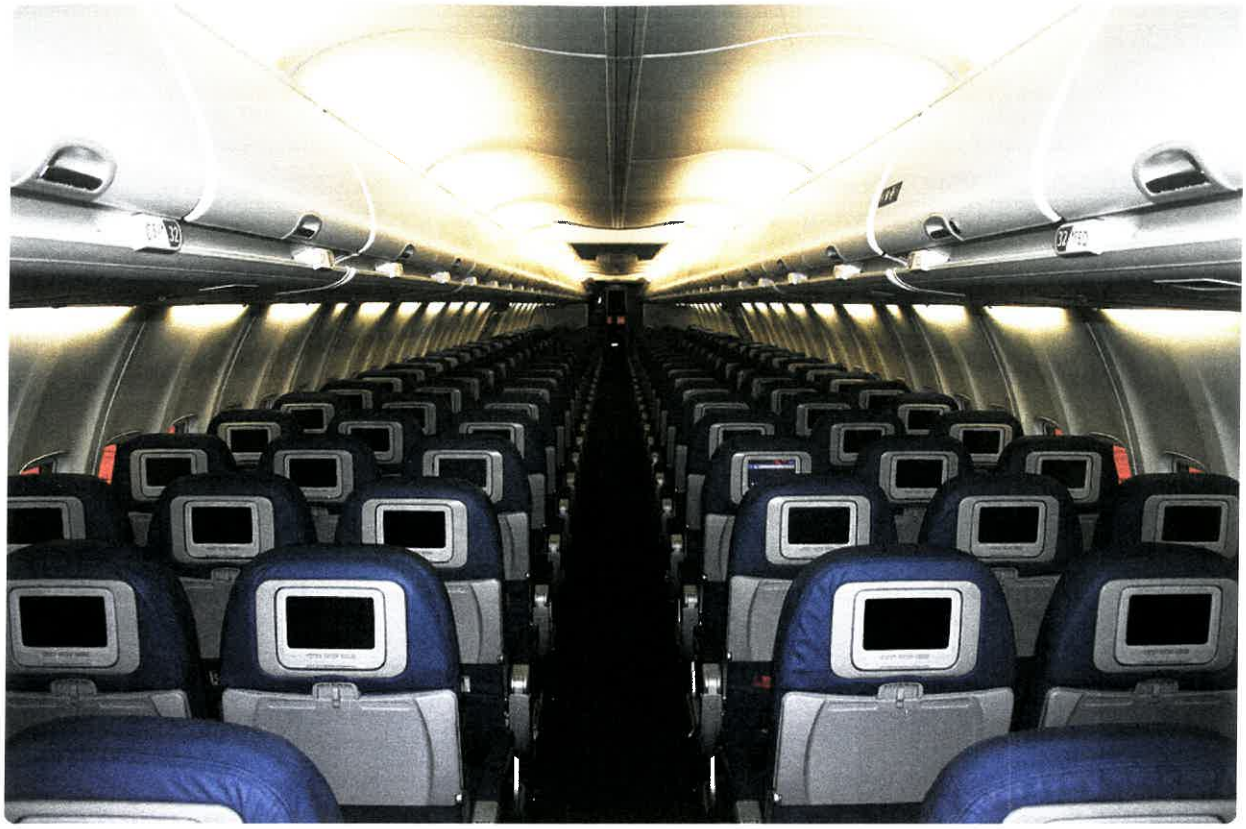


Figure 10-16. IFE system installed on a Boeing 737-800.

Question: 10-1
Explain the physical construction of a fiber optic cable.

Question: 10-2
What are the advantages and disadvantages of fiber optics over copper wire?

Question: 10-3
Describe the components of a fiber optic data bus and how it operates.

Question: 10-4
What is the difference between multimode and single-mode fiber optic cable?

Question: 10-5
What is key to ensure that fiber optic terminations couple light from one component to another with as little loss of optical power as possible?

Question: 10-6
What is the advantage of a star coupler over a T-coupler?

Question: 10-7
What is Pulse-Coded Modulation (PCM)?

Question: 10-8
Compare and contrast NRZ (non-return-to-zero) code to Manchester code.

ANSWERS

Answer: 10-1
A fiber optic cable consists of the core, which is a thin glass or plastic center where the light travels, surrounded by an outer optical material, called a cladding, which reflects the light back into the core, and a black polyurethane outer jacket over the cladding to protect the cable from damage and moisture. A plastic coating applied to the cladding, called a buffer jacket, provides additional protection. Materials made from fiberglass or Kevlar add mechanical strength to the cable.

Answer: 10-2
Besides having a high data-rate capability and a wide bandwidth to carry more information, optical buses exhibit extremely low loss and low crosstalk since there is no line capacitance or mutual coupling. Optical cables are immune from electro-magnetic interference (EMI) and can withstand nuclear radiation. All though optical cables are lighter than copper cables, they are generally more expensive and are more difficult to splice than copper wires.

Answer: 10-3
A fiber optic link connects two electrical circuits from the data source to the data sync using a light source, transmitter, fiber optic cable, and receiver. The light source will be either a LED or laser diode. The transmitter converts electrical signals into light pulses and sends the pulses over the fiber optic cable to the receiver. A fiber optic receiver consists of a photocell detector, amplifier, and output circuit. The receiver decodes the light pulse and converts the signals back to their original electrical state.

Answer: 10-4
Many beams of light travel through the multimode cable bouncing off of the cable walls. Attenuation is caused by the scattering and absorption of light as it travels down the fiber core. Single-mode fiber uses a single direct beam of light, thus allowing for greater distances and increased transfer speeds without suffering from scattering and absorption losses.

Answer: 10-5
The key to low loss is precise alignment of the mated fiber cores so that nearly all the light is coupled from one fiber across the junction to the other fiber. Fibers must be checked for precise perpendicularity and end finish prior to termination. Mismatches can occur due to variations in tolerances between the diameter and concentricity of the core and cladding. In addition, connectors and splices can contribute to insertion losses due to variations in lateral displacement, end separation, angular misalignment and surface roughness.

Answer: 10-6
A star coupler has multiple ports to distribute the optical power point-to-point to multiple terminals. Unlike, the tee coupler, the insertion loss does not increase directly with the number of terminals; and therefore, it is well suited for connecting a large number of terminals to the fiber optic network.

Answer: 10-7
A modulation code is used as a method of encoding digital data such that turning the source on and off forms Pulse-Coded Modulation (PCM) waveforms that correspond to binary number equivalents.

Answer: 10-8
NRZ is a non-self-clocking code whereby the signal remains high during a string of 1s and remains low for a sting of 0s. Manchester Code is a self-clocking code whereby there is a transition in the middle of each bit period. As such, for a binary 1, the first half of the period is high, and the second half is low. For a binary 0, the first half is low and the second half is high. As a result, Manchester code has two symbols per bit, instead of one as in NRZ code.

Question: 10-9
Explain the concept of Wavelength-Division Multiplexing (WDM).

Question: 10-10
What are the advantages and disadvantages of laser diodes versus LEDs?

Question: 10-11
What is the purpose of using photodiodes inside the laser diode cell?

Question: 10-12
Explain the concept of optical resonance.

Question: 10-13
What determines the performance of a fiber-optic receiver?

Question: 10-14
Explain the operation of a Photo-Diode Detector.

ANSWERS

Answer: 10-9
By using elements, such as gallium, arsenic, and phosphorous, an Light-Emitting Diode (LED) can be designed to radiate different colors, such as red, green, yellow and blue light. Different color LEDs can be employed in the transmitter to signify which receiver the signal is intended. Light that is emitted by a semiconductor can be absorbed by the same semiconductor material in the receiver. WDM is used in some fiber optic data bus systems whereby the selection of the color of light passing through a fiber cable denotes the source and destination address.

Answer: 10-10
In general, laser diodes have higher modulation bandwidth, greater optical output power, and higher coupling efficiency to the fiber cable, and therefore, are widely used for high-speed digital applications. The reason why a laser diode has a higher coupling efficiency is due to its narrow spatial beam width. The only disadvantage is that they cost more than an LED.

Answer: 10-11
Photodiodes are often installed on the rear face of the cavity to monitor the light output to adjust the drive current to maintain a constant optical power level.

Answer: 10-12
Lasing is achieved through optical resonance whereby photons are generated due to a high current being applied across the semiconductor material. These photons interact with more incoming electrons, helping to produce more photons, and so on in a self-perpetuating process called optical resonance.

Answer: 10-13
Receivers are classified based on their sensitivity and dynamic range. Sensitivity specifies the weakest optical signal that can be detected while rejecting noise. Dynamic range is the difference between the minimum and the maximum power levels. The minimum level is determined by receiver sensitivity and the maximum level is determined by the gain setting on the amplifier.

Answer: 10-14
When a photon strikes a semiconductor atom, it raises the energy level above what is needed to hold its electrons in orbit. The extra energy frees an electron enabling it to flow as current. The vacated position of the electron becomes a hole. In photodiodes, this occurs in the depletion area of the reversed biased PN (positive-negative) junction turning on the device and allowing current to flow.

DIGITAL TECHNIQUES ELECTRONIC INSTRUMENT SYSTEMS

ELECTRONIC DISPLAYS

SUB-MODULE 11

PART-66 SYLLABUS LEVELS

CERTIFICATION CATEGORY → B2

Sub-Module 11

ELECTRONIC DISPLAYS

Knowledge Requirements

5.11 - Electronic Displays	
Principles of operation of common types of displays used in modern aircraft, including Cathode Ray Tubes, Light Emitting Diodes and Liquid Crystal Display.	2

5.11 - ELECTRONIC DISPLAYS

As previously stated, "glass cockpits" that evolved in the early 1970's were more much more reliable than mechanical or electro-mechanical analog instruments, and had the advantage of combining several flight and navigation functions into one display to provide the crew with greater situational awareness. Initially, glass cockpits used Cathode Ray Tube (CRT) technology.

CATHODE RAY TUBES

As shown in ***Figure 11-1***, a CRT is a vacuum tube with an electron gun that sends a beam of electrons to a fluorescent screen. The electrons are accelerated through a hole in the anode by the voltage difference between the cathode and the anode. The electron beam is steered by horizontal and vertical defection plates on to any position on the screen. The electron beam striking the phosphor on the screen causes this point on the screen to emit light. The light intensity is controlled by changing the anode voltage, which can be as high as 20 000 volts.

In a color display, the screen is coated with a pattern of phosphor dots doped to emit three primary colors: Red, Green, and Blue (RGB). Three electron guns, one for each color, converge on a thin foil shadow mask with holes aligned to a RGB phosphor dot triad, which forms a pixel (picture element). The combination of these three primary colors can produce any number of colors and hues depending on the intensity of each electron beam on their respective pixels. (***Figure 11-2***)

The image on the CRT is made by sweeping the electron beam horizontally from left to right, one line after the other. The display resolution varies depending on the number of lines. For example, a display resolution of 1024 × 768 means that the screen width is 1024 pixels and the height is 768 pixels for a total of 786 432 pixels. The human eye will not notice the flicker of the image if the image changes at least every 30 milliseconds. Therefore, CRTs typically have a 60 Hz refresh rate meaning that the screen is updated every 1⁄60 of a second or 16.7 milliseconds.

This line-by-line scanning technique common in everyday television CRTs is known as raster. Raster is well suited for quickly filling in the background for artificial horizon, digital map and weather radar display formats. However, cockpit displays also use a technique called stroke or vector graphics to precisely draw symbology overlaid on the raster background. With stroke graphics, the display is sent voltage point pairs and a beam draws a line in one stroke from the last point to the current point. The display processor generates the points that define the shape to send to the display and a Digital-to-Analog Converter (DAC) converts these digital signal points to voltages for the CRT.

LIGHT EMITTING DIODES

Due to their large volume, weight, and power requirements, vacuum tube CRT displays have largely been displaced by solid-state displays, such as Light Emitting Diodes and Liquid Crystal Displays.

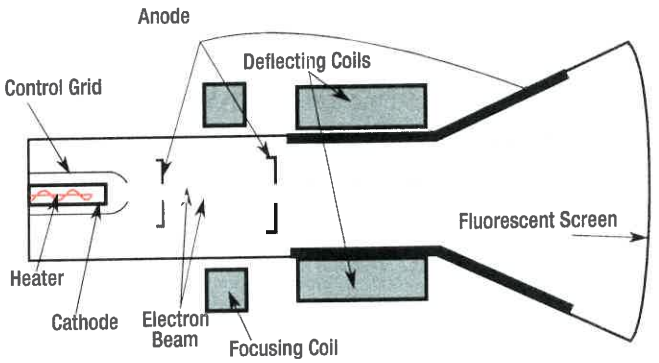


Figure 11-1. Operation of a cathode ray tube.

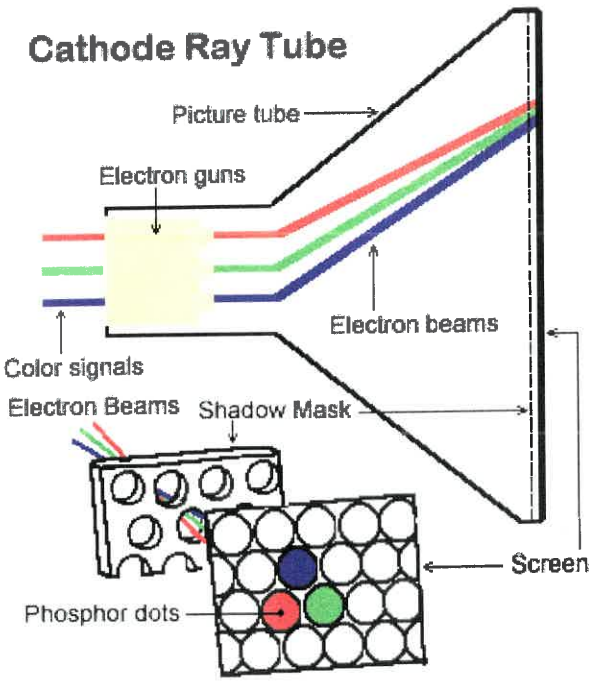


Figure 11-2. Color CRT has 3 electron guns and RGB phosphor dots.

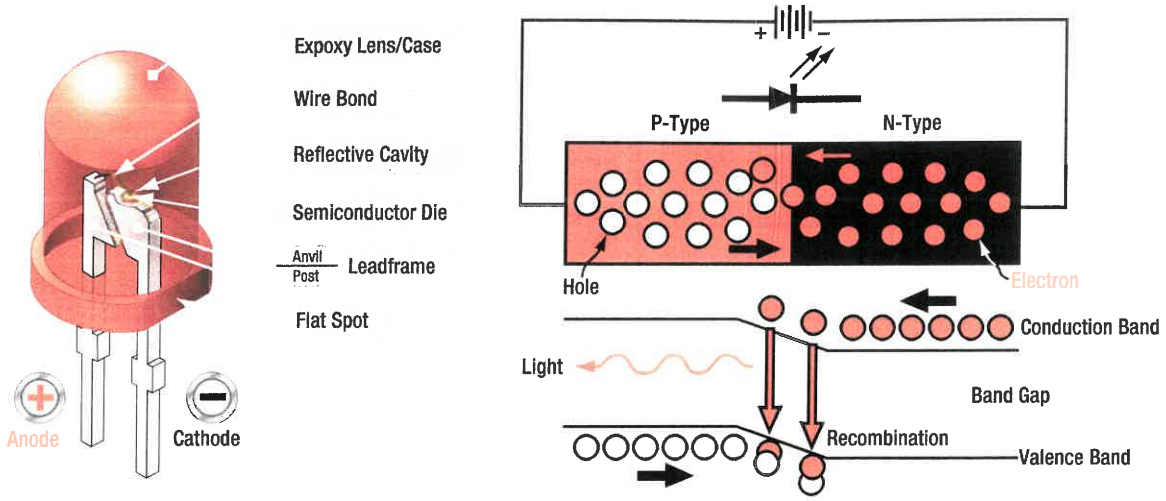


Figure 11-3. An LED producing light by electrons dropping into holes and giving off energy.

Light Emitting Diodes (LEDs) operate on the principle of electroluminescence, which is a term used to describe a phenomenon whereby light emission is caused by the application of an electric current. Light contains electromagnetic energy that is carried by photons. The amount of energy depends on the frequency of light of the photon. This energy can be very useful in the operation of electronic devices since all semiconductors are affected by light energy. LEDs are used for indicator lights, digital readouts, backlighting of liquid crystal display screens, and light sources for fiber optic transmitters. As a cockpit display, LEDs have very good brightness and contrast; however, their resolution is limited to only about 64 cells per inch.

LEDs are simple and reliable. They are constructed of semiconductor material. When a free electron from a semiconductor drops into a semiconductor hole, energy is given off. This is true in all semiconductor materials. However, the energy released when this happens in certain materials is in the frequency range of visible light. ***Figure 11-3*** illustrates the anatomy of a single LED, the symbol of an LED, and a graphic depiction of the LED process. Note that when the diode is reversed biased, no light is given off. However, when the diode is forward biased, the energy given off is visible in the color characteristic for the material being used. ***Figure 11-4*** is a table that delineates common LED colors and the semiconductor material that is used in the construction of the diode.

As stated in the previous Sub-Module, a fiber optic transmitter has an LED source and a fiber optic receiver contains a photodiode detector, which converts the light back into an electrical signal. When a photon strikes a semiconductor atom, it raises the energy level above what is needed to hold its electrons in orbit. The extra energy frees an electron enabling it to flow as current. The vacated position of the electron becomes a hole. In photodiodes, this occurs in the depletion area of the reversed biased PN (positive-negative) junction turning on the device and allowing current to flow. ***Figure 11-5*** illustrates a photodiode in a coil circuit. In this case, the light striking the photodiode causes current to flow in the circuit whereas the diode would have otherwise blocked it. The result is the coil energizes and closes another circuit enabling its operation.

LIQUID CRYSTAL DISPLAYS

CRTs and LEDs are emissive displays in that they both generate their own light. However, Liquid Crystal Displays (LCDs) are non-emissive in that they require an external light source to operate. Liquid crystals consist of molecules that are elongated or rod-shaped. When the crystals are placed on a surface that has a pattern of parallel grooves, the elongated molecules will align themselves with the grooves. An LCD cell is constructed by placing the crystals between two grooved glass plates where the grooves on the top plate are aligned 90 degrees perpendicular to the bottom plate. This causes the liquid crystals to twist as they move from top to bottom.

The LCD cells are sandwiched between two glass polarizer plates with a fluorescent light source behind one of the plates. If the two polarizers were oriented in the same direction, light would pass through. However, if the two polarizer plates are placed orthogonal to each

Color	Wavelength (nm)	Voltage (V)	Semiconductor Material
Infrared	$\lambda > 760$	$\Delta V < 1.9$	Gallium arsenide (GaAs) Aluminium gallium arsenide (AlGaAs)
Red	$610 < \lambda < 760$	$1.63 < \Delta V < 2.03$	Aluminium gallium arsenide (AlGaAs) Gallium arsenide phosphide (GaAsP) Aluminium gallium indium phosphide (AlGaInP) Gallium(III) phosphide (GaP)
Orange	$590 < \lambda < 610$	$2.03 < \Delta V < 2.10$	Gallium arsenide phosphide (GaAsP) Aluminium gallium indium phosphide (AlGaInP) Gallium(III) phosphide (GaP)
Yellow	$570 < \lambda < 590$	$2.10 < \Delta V < 2.18$	Gallium arsenide phosphide (GaAsP) Aluminium gallium indium phosphide (AlGaInP) Gallium(III) phosphide (GaP)
Green	$500 < \lambda < 570$	$1.9[32] < \Delta V < 4.0$	Indium gallium nitride (InGaN) / Gallium(III) nitride (GaN) Gallium(III) phosphide (GaP) Aluminium gallium indium phosphide (AlGaInP) Aluminium gallium phosphide (AlGaP)
Blue	$450 < \lambda < 500$	$2.48 < \Delta V < 3.7$	Zinc selenide (ZnSe) Indium gallium nitride (InGaN) Silicon carbide (SiC) as substrate Silicon (Si) as substrate — (under development)
Violet	$400 < \lambda < 450$	$2.76 < \Delta V < 4.0$	Indium gallium nitride (InGaN)
Purple	Multiple Types	$2.48 < \Delta V < 3.7$	Dual blue/red LEDs, blue with red phosphor, or white with purple plastic
Ultraviolet	$\lambda < 400$	$3.1 < \Delta V < 4.4$	diamond (235 nm)[33] Boron nitride (215 nm)[34][35] Aluminium nitride (AlN) (210 nm)[36] Aluminium gallium nitride (AlGaN) Aluminium gallium indium nitride (AlGaInN) — (down to 210 nm)[37]
White	Broad Spectrum	$\Delta V = 3.5$	Blue/UV diode with yellow phosphor

Figure 11-4. LED colors and the materials used to construct them.

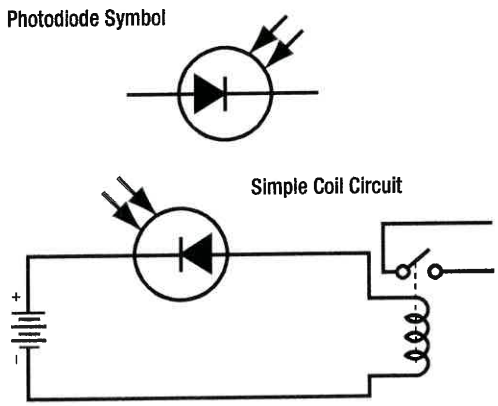


Figure 11-5. A photodiode in a simple coil circuit.

other, the light would be blocked from passing, if not for the liquid crystals that twist the light as it passes through the cell. As shown in ***Figure 11-6***, when light is applied to the left polarizer with the light projected parallel to its grooves, the polarization rotates by 90 degrees through the twisted liquid crystals, thereby allowing light to pass through the right polarizer that is aligned orthogonal to the left polarizer.

However, when an electric force field is applied to the liquid crystal cell in a direction normal to the cell's grooved surfaces, the molecules will align with the field and the twisting effect will be destroyed. The result is that there will be no polarization, and therefore, the light will be blocked from passing through the right polarizer - the cell will appear black.

As shown in ***Figure 11-7***, the electric field is applied by electrodes that are sandwiched on either side of the liquid crystal. By controlling the voltage applied across the liquid crystal layer in each pixel, various amount of light can be allowed to pass thus constituting

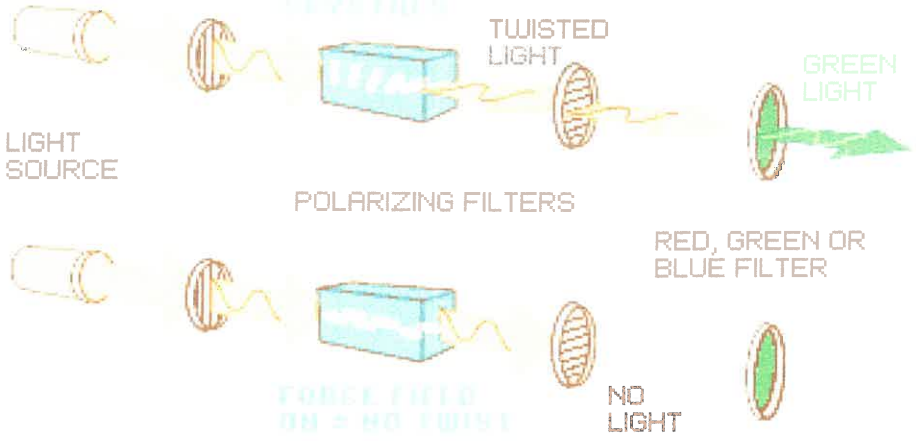


Figure 11-6. Twisted liquid crystals allow light to flow through the right polarizer.

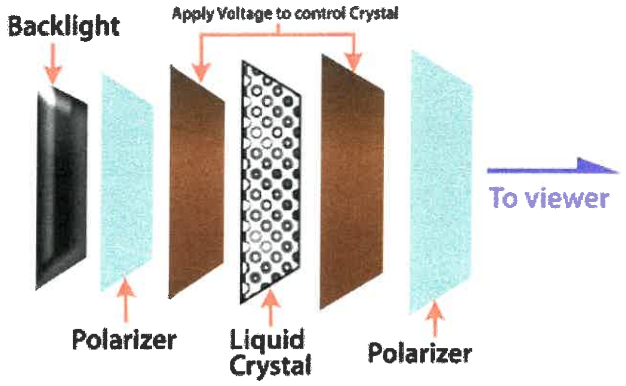


Figure 11-7. Basic liquid crystal cell.

different shades of gray or various levels of brightness. In addition, RGB filters can be inserted between the liquid crystal and the outside polarizer to form color displays.

ACTIVE MATRIX LIQUID CRYSTAL DISPLAY

A liquid crystal display made of a matrix of cells as described above is what is known as passive-matrix LCD technology whereby a pixel is turned on or off at the intersection of each row and column in the matrix to display information. This technology is suitable for low quality displays, but for Electronic Instrument Systems that require higher resolution, Active-Matrix Liquid Crystal Display (AMLCD) technology is more commonly used. AMLCDs are considerably more sophisticated, and thus more expensive, because a Thin-Film Transistor (TFT) switch is integrated on the electrode panel for each and every pixel. Since the transistors are individually controlled, the switching speed and response time is much greater, thus the contrast ratio is greatly improved.

As illustrated in ***Figure 11-8***, one side of the liquid crystal has a transparent indium tin oxide (ITO) electrode that is common for all pixels. The TFTs connect the pixels to power from the data line when they are turned on. Just as in passive-matrix LCDs, the image information is sent one line at a time. By choosing different levels of bias it is possible to have many shades of gray or many intensities of color. Color displays have three times the pixels in the horizontal direction as monochrome displays, thus a 640 × 380 display actually has 1920 × 480 pixels.

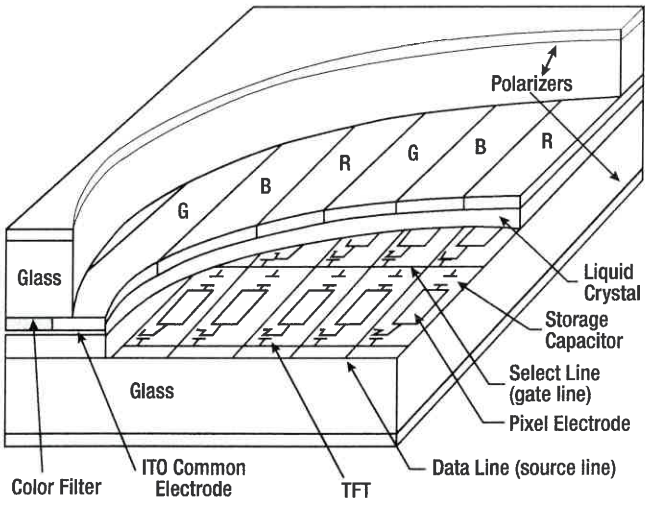


Figure 11-8. Cut-away view of an AMLCD.

Question: 11-1
Explain the operation of a Cathode Ray Tube (CRT) display.

Question: 11-2
How are colors generated in a Cathode Ray Tube (CRT) display?

Question: 11-3
What is the difference between raster scan and stroke scan?

Question: 11-4
Explain the operation of a Light Emitting Diode (LED).

Question: 11-5
Explain how liquid crystals behave when an electric field is applied.

Question: 11-6
What is the difference between a passive-matrix Liquid Crystal Display (LCD) and an active-matrix LCD in both operation and performance?

ANSWERS

Answer: 11-1
A CRT is a vacuum tube with an electron gun that sends a beam of electrons to a fluorescent screen. The electrons are accelerated through a hole in the anode by the voltage difference between the cathode and the anode. The electron beam is steered by horizontal and vertical defection plates on to any position on the screen. The electron beam striking the phosphor on the screen causes this point (pixel) on the screen to emit light. The light intensity is changed by changing the anode voltage.

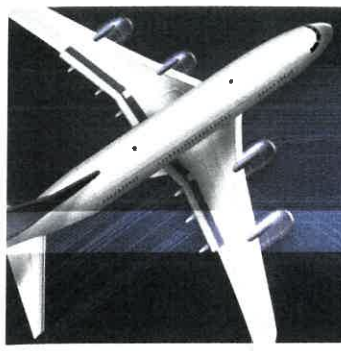
Answer: 11-2
In a color display, the screen is coated with a pattern of phosphor dots doped to emit three primary colors: Red, Green, and Blue (RGB). Three electron guns, one for each color, converge on a thin foil shadow mask with holes aligned to a RGB phosphor dot triad, which forms a pixel. The combination of these three primary colors can produce any number of colors and hues depending on the intensity of each electron beam on their respective pixels.

Answer: 11-3
Raster line-by-line scanning is well suited for quickly filling in the background for artificial horizon, digital map and weather radar display formats. However, cockpit displays also use a technique called stroke or vector graphics scanning to precisely draw symbology overlaid on the raster background. With stroke graphics, the display is sent voltage point pairs and a beam draws a line in one stroke from the last point to the current point.

Answer: 11-4
LEDs operate on the principle of electroluminescence, which is a term used to describe a phenomenon whereby light emission is caused by the application of an electric current. When a free electron from a semiconductor drops into a semiconductor hole, energy is given off. When the diode is forward biased, the energy given off is visible in the color characteristic for the material it is made of.

Answer: 11-5
When light is applied to one of the polarizers with the light projected parallel to its grooves, the polarization rotates by 90 degrees through the twisted liquid crystals, thereby allowing light to pass through the other polarizer. However, when an electric force field is applied to the liquid crystal cell in a direction normal to the cell's grooved surfaces, the molecules will align with the field and the twisting effect will be destroyed. The result is that there will be no polarization, and therefore, the light will be blocked from passing through the polarizer and the cell will appear black.

Answer: 11-6
With passive-matrix LCDs, a pixel is turned on or off at the intersection of each row and column in the matrix to display information. Active-Matrix Liquid Crystal Displays (AMLCD) are considerably more sophisticated, and thus more expensive, because a Thin-Film Transistor (TFT) switch is integrated on the electrode panel for each and every pixel. Since the transistors are individually controlled, the switching speed and response time is much greater, thus the contrast ratio is greatly improved.



DIGITAL TECHNIQUES ELECTRONIC INSTRUMENT SYSTEMS

ELECTROSTATIC SENSITIVE DEVICES

SUB-MODULE 12

PART-66 SYLLABUS LEVELS

CERTIFICATION CATEGORY → B2

Sub-Module 12

ELECTROSTATIC SENSITIVE DEVICES

Knowledge Requirements

5.12 - Electrostatic Sensitive Devices

Special handling of components sensitive to electrostatic discharges;	2
Awareness of risks and possible damage, component and personnel anti-static protection devices.	

5.12 - ELECTROSTATIC SENSITIVE DEVICES

Static electricity is a simple fact of nature. It is around us all the time and is caused by friction. Most work environments have non-conductive floors and no means of controlling the humidity. As the humidity drops below 20%, a static charge builds up on a person's body. The faster the person walks, the higher the charge. Simply walking across a carpet can generate 1 500 volts of static electricity at 65% relative humidity and up to 35 000 volts of static electricity at 20% relative humidity. Plastics used in most products will produce charges from 5 000 to 10 000 volts. Once the person sits down at the work station, the electrostatic field surrounding their body is enough to cause damage to sensitive electronic components without even touching them. However, when the person touches the component, an electrostatic discharge or spark occurs, and zap, the component is most certainly destroyed. (***Figure 12-1***)

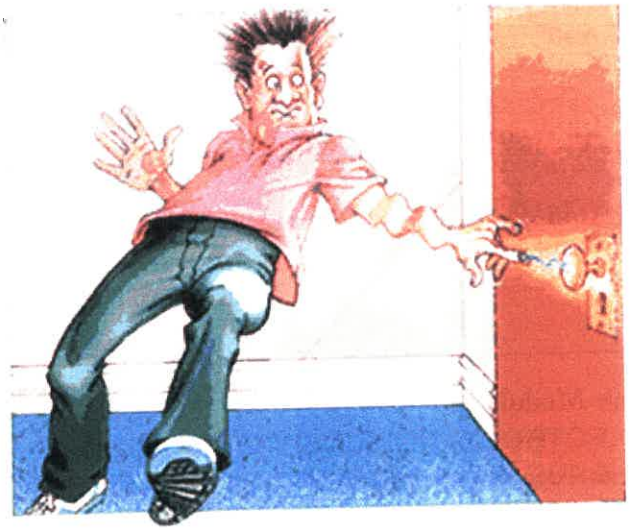


Figure 12-1. Electrostatic discharge.

RISKS AND POSSIBLE DAMAGE

Electro-Static Discharge (ESD) is defined in U.S. military handbook DOD-HKBK-263 as "transfer of electrostatic charges between bodies at different potentials caused by direct contact or induced by an electrostatic field". In other words, an electrostatic charge on one body can be imparted to another body through induction from an electromagnetic field, or through conduction via physical contact. If an electronic component that is charged is then suddenly grounded, the charge will dissipate to ground, but in the process, the component will be damaged due to excessive heat from breakdown of the dielectric material within the component.

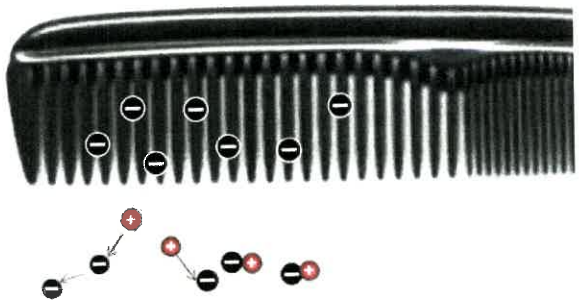


Figure 12-2. Electrostatic induction.

Electrostatic induction occurs when a charged object induces the redistribution of charges in another object. A classic example of this is picking up pieces of paper using a comb that was rubbed against fur. In ***Figure 12-2***, the comb is charged negative, meaning that there exists an excess of electrons built up on the comb. The side of the paper closest to the comb will end up being slightly positive due to the attraction of opposite charges, while the opposite side of the paper will be slightly negative due to the repulsion of similar charges.

MIL-STD-1686C is the U.S. military standard for "ESD control programs for the protection of electrical and electronic parts, assemblies, and equipment". It recognizes two classes of ESD-sensitive items: Class I for 100 to 1 000 volts and Class II for 1 001 to 4 000 volts sensitivity. Most electronic components are in Class I. For example, bi-polar transistors are susceptible to ESD between 380 to 7 000 volts; CMOS devices are susceptible between 250 volts and 3 000 volts; and EPROMs, used in computer memories, are susceptible to as low as 100 volts.

The ESD issue is not going away. In fact, the problem is getting much worse. As component technology continues to advance to achieve higher speeds and greater functionality, their physical geometries are shrinking, which is causing components to become even more susceptible to lower discharge voltages. The following section will discuss special handling of ESD-sensitive components and anti-static protection devices which must be used to protect these sensitive electronic components from the dangers of electrostatic discharge.

ANTI-STATIC PROTECTION

CONTROLLED ENVIRONMENT

Static electricity can't be eliminated. It can only be controlled. Therefore, it is essential to only handle ESD sensitive devices in static-safe controlled environment. Signage must be placed outside any ESD controlled areas to warn people that special precautions must be taken before entering the controlled environment. (***Figure 12-3***) Any insulating materials, such as nylon, mylar, vinyl, rubber, mica, ceramics, fiberglass, wood, styrofoam, and plastic, will store static electricity, and therefore, should be kept out of the work area. Technicians should only enter the work area wearing anti-static (steel mesh) smocks and conductive (leather-soled) footwear. If wearing an anti-static heel strap in place of conductive shoes, the grounding cord must run into the sock in order to make contact with the skin.

Figure 12-3. Warning sign for an ESD controlled area.

STATIC-SAFE WORKSTATION

Conductive materials, including personnel, must be grounded. The floor surface should be covered with conductive paints or coatings, anti-static floor finishes, or anti-static vinyl flooring. As shown in ***Figure 12-4***, the work station should have a static dissipative floor mat and table-top mat that have a surface resistivity of 105 to 1 012 ohms per square inch. The conductive mat not only provides a surface that is free of static charge on which to work, but must also remove the static charge from conductive items placed on it. Both the floor and table-top mats should be connected through a 1 mega-ohm resistor connected to a common ground point. The resistor is required to protect personnel in the event the ground becomes electrically live.

Figure 12-4. Static-safe workstation.

ANTI-STATIC WRIST STRAPS

The same safety requirement holds true for the anti-static wrist strap (***Figure 12-5***) in that the coil cord must be plugged or clipped into a receptacle with a 1 mega-ohm resistor connected to a common ground point. The wrist strap must be secure around the wrist at all times while seated at the work station so that it makes good electrical connection with the skin to dissipate any electrical charge to ground before touching sensitive electronic components.

Figure 12-5. Anti-static electricity grounding wristband.

GROUNDING TEST STATIONS

All anti-static devices should be tested before entering the static-safe controlled environment. ***Figure 12-6***

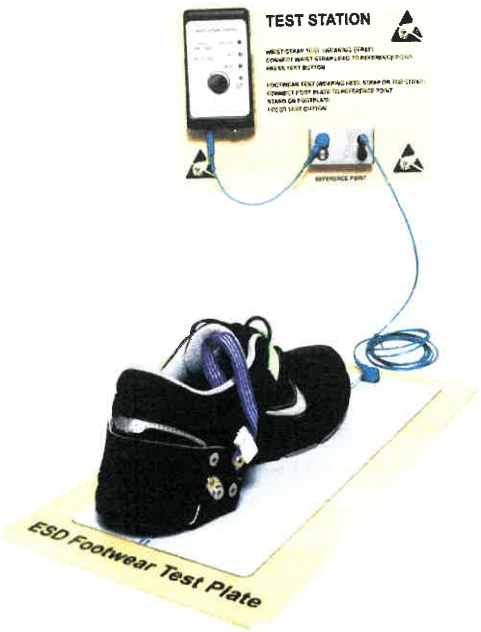


Figure 12-6. Typical grounding test station.

is a picture of a typical grounding test station used to determine whether the anti-static devices are working properly. A green indicator light means that the wrist strap is worn properly and is working as intended. The test station can also be used to test footwear, heal straps, and coil cords as well.

IONIZERS

Since it is not practical to raise the relative humidity to high levels due to operator discomfort and the fact that it would cause metals to rust, the controlled environment should be equipped with ionizers to neutralize any charged insulators commonly found in the work environment. Because positively or negatively charged surfaces will attract ions of the opposite charge, an air stream containing both positive and negative ions is used to neutralize the charged surface. Once the surface is neutralized, it remains so as long as the ion stream is present. Ionizers are available in high-pressure, low-volume air guns for periodic localized cleaning, and low-pressure, high-volume wall-mounted units designed to be suspended over the work station with the ionized air blowing down over the area to be protected against an ESD event. (***Figure 12-7***)

Designed to cover a work station area, the ionizer will neutralize even the highest electrostatic charge. Normally the system is mounted 30"-36" above the area to be controlled, producing a balanced ionization pattern of approximately 36" wide × 48" long. It is highly recommended to use an electrostatic field meter to detect static charges in the work area to be assured that the ionizer is functioning properly before handling sensitive components. If the ionizer is not working properly, topical anti-stats should be sprayed in the work area to control the generation and accumulation of electrostatic charges.

SPECIAL HANDLING

All ESD sensitive components should transported in a closed conductive container (e.g., LRU or a tote box). The container must be stored on a grounded rack, and when moved to the work station, it must make contact with the grounded table mat. Any accumulated charge on the human body should first be discharged, by wearing the grounded anti-static wrist strap, before opening the protective container containing the ESD sensitive component. Also, always use a grounded soldering iron to install ESD sensitive components.

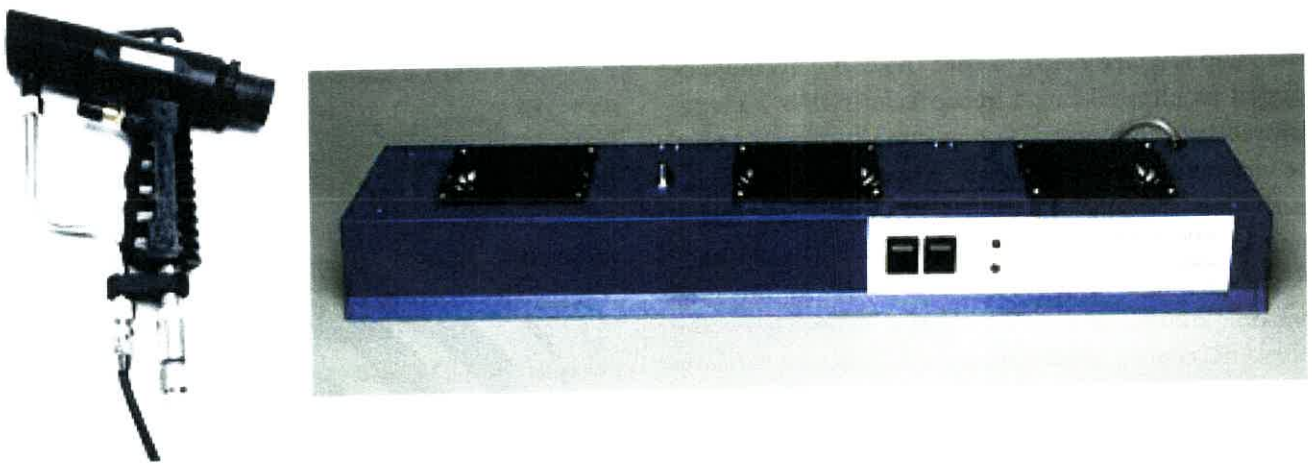


Figure 12-7. Hand-held and wall-mounted ionizers.

All ESD sensitive components should be packaged is an electrostatic shielded conductive bag. These laminated bags (***Figure 12-8***) are made from an outer layer of transparent metallic sheeting or an aluminum foil material, a middle insulation layer, and an inner anti-static layer. Finally, the bag is sealed with a label warning that there is an ESD sensitive component inside.

Figure 12-8. Laminated metalized bag for storing ESD sensitive components.

Question: 12-1
What causes static electricity and electrostatic induction?

Question: 12-2
What is Electro-Static Discharge (ESD) and what are the ways that it can damage electronic components?

Question: 12-3
How susceptible are electronic components to damage from ESD?

Question: 12-4
What precautions must be taken when working in an ESD controlled environment?

Question: 12-5
How does one maintain a static-free workstation?

Question: 12-6
What is the reason for using ionizers?

Question: 12-7
What precautions should be used when handling ESD sensitive components?

ANSWERS

Answer: 12-1
Static electricity is caused by friction. Simply walking across a carpet can generate 1 500 volts of static electricity at 65% relative humidity and up to 35 000 volts of static electricity at 20% relative humidity. Electrostatic induction occurs when a charged object induces the redistribution of charges in another object.

Answer: 12-2
ESD is the transfer of electrostatic charges between bodies at different potentials caused by direct contact or induced by an electrostatic field. If an electronic component that is charged is then suddenly grounded, the charge will dissipate to ground, but in the process, the component will be damaged due to excessive heat and/or from breakdown of the dielectric material within the component.

Answer: 12-3
Bi-polar transistors are susceptible to ESD between 380 to 7 000 volts; CMOS devices are susceptible between 250 volts and 3 000 volts; and EPROMs, used in computer memories, are susceptible to as low as 100 volts.

Answer: 12-4
Any insulating materials, such as nylon, mylar, vinyl, rubber, mica, ceramics, fiberglass, wood, styrofoam, and plastic, will store static electricity, and therefore, should be kept out of the work area. Technicians should only enter the work area wearing anti-static (steel mesh) smocks and conductive (leather-soled) footwear.

Answer: 12-5
The work station should have a static dissipative floor mat and table-top mat that are connected through a 1 mega-ohm resistor to a common ground point. The wrist strap must be secure around the wrist at all times while seated at the work station so that it makes good electrical connection with the skin to dissipate any electrical charge to ground before touching sensitive electronic components. The wrist strap cord must be plugged into a receptacle with a 1 mega-ohm resistor connected to the same common ground point.

Answer: 12-6
A controlled environment should be equipped with ionizers to neutralize any charged insulators commonly found in the work environment. Because positively or negatively charged surfaces will attract ions of the opposite charge, an air stream containing both positive and negative ions is used to neutralize the charged surface. Once the surface is neutralized, it remains so as long as the ion stream is present.

Answer: 12-7
All ESD sensitive components should transported in a closed conductive container (e.g., LRU or a tote box). The container must be stored on a grounded rack, and when moved to the work station, it must make contact with the grounded table mat. Any accumulated charge on the human body should first be discharged, by wearing the grounded anti-static wrist strap, before opening the protective container containing the ESD sensitive component. All ESD sensitive components should be packaged is an electrostatic shielded conductive bag.

SUB-MODULE 13

PART-66 SYLLABUS LEVELS

CERTIFICATION CATEGORY → B2

Sub-Module 13

SOFTWARE MANAGEMENT CONTROL

Knowledge Requirements

5.13 - Software Management Control

Awareness of restrictions, airworthiness requirements and possible catastrophic effects of unapproved changes to software programs.	2

5.13 - SOFTWARE MANAGEMENT CONTROL

RESTRICTIONS AND CATASTROPHIC EFFECTS

As a result of advances in digital electronics, modern aircraft have become very sophisticated with many millions of lines of code running simultaneously in dozens of airborne computers. As such, it has become imperative that software management control includes a thorough definition and documentation of the aircraft software development process in order to avoid catastrophic effects of unapproved software changes being uploaded onboard aircraft computers that could cause aircraft loss and multiple fatalities. Imagine the consequences if during an Instrument Flight Rules (IFR) approach in zero visibility, the flight control software failed.

Besides the basic production of source code and executable object code, safety standards must be adhered to that specify required software documentation and life cycle artifacts, such as an airworthiness certification plan, software quality assurance plan, software configuration management plan, configuration control procedures, software code standard, software design standard, software requirements standard, software development plan, software verification plan, software design document, software requirements document, traceability, test cases and test procedures, verification results, quality assurance records, configuration management records, problem reports, and a software accomplishments summary.

AIRWORTHINESS REQUIREMENTS

"Software Considerations in Airborne Systems and Equipment Certification" is a standards document dealing with the safety of software used in aircraft systems. It was jointly published in 1992 by the Radio Technical Commission for Aeronautics (RTCA) as DO-178B, and by the European Organization for Civil Aviation Equipment (EUROCAE) as ED-12B. The Federal Aviation Administration (FAA) and European Aviation Safety Agency (EASA) have used DO-178B/ED-12B as certification guidance to determine if the software will perform reliably in aircraft systems.

DO-178B/ED-12B established design assurance levels based on a safety assessment process and hazard analysis by examining the effects of a failure condition in each aircraft system. There are five criticality levels defined in terms of the potential consequence of an undetected error in the software as certified at each of the following levels:

- **Level A**: Catastrophic: Prevents continued safe flight or landing. Failure may cause multiple fatalities and loss of aircraft.
- **Level B**: Hazardous/Severe: Failure has large negative impact on safety or performance. May cause serious or fatal injuries to a smaller number of passengers.
- **Level C**: Major: Failure significantly reduces safety margin, impairs crew efficiency, discomfort or possible injuries to passengers.
- **Level D**: Minor: Failure reduces the aircraft safety margins, but well within crew capabilities. May include passenger inconvenience such as a routine flight plan change.
- **Level E**: No Effect: Failure has no impact on the safety or aircraft operation.

Flight control and navigation systems are flight critical and thus require Level A certification. Cabin entertainment systems fall at the other end of the criticality spectrum and would be considered as Level E systems (except for the crew's ability to override it when making public address announcements). Typically, different levels of software criticality will not be run on the same processor, unless of course, an approved software partitioning scheme, such as ARINC 653, is employed. ARINC 653 (Avionics Application Standard Software Interface) is a software specification for space and time partitioning in a real-time operating system that allows a processor to host multiple software applications of different criticality levels on the same processor. ARINC 653 is used in Integrated Modular Avionic (IMA) systems.

When DO-178B was initially published, most software was coded by hand. However, software development processes have since evolved to automatic coding using model-based design. As such, there was a need for clarification or refinement of the definitions between high-level system requirements and low-level

software requirements. Also required was a process to determine how to verify software that was model-based and determine if model-based simulation or formal methods could replace some or all of the software testing activities. Hence, a new standard, DO-178C was developed in 2011 to replace DO-178B. In July of 2013, the FAA released an Advisory Circular (AC 20-115C) making DO-178C as recognized "compliance with applicable airworthiness regulations for the software aspects of airborne systems".

The newer DO-178C standard contains several supplements that map closely with current industry software development and verification practices: Software Tool Qualifications (DO-330), Model-Based Development and Verification (DO-331), Object-Oriented Technology (DO-332), and Formal Methods (DO-333). Software development tools such as MATLAB, Simulink, and Embedded Coder, are widely used to support software development activities involving model-based design in compliance with DO-178C.

Figure 13-1 is a diagram illustrating the required tracing between certification artifacts as required by DO-178C. Red traces are required only for Level A software applications. Purple traces are required for Levels A, B and C. Green traces are required for Levels A through D. Level E does not require any traceability due to its non-critical nature. DO-178C states that Level A executable object code must be "robust with respect to the software requirements that it can respond correctly to abnormal inputs and conditions".

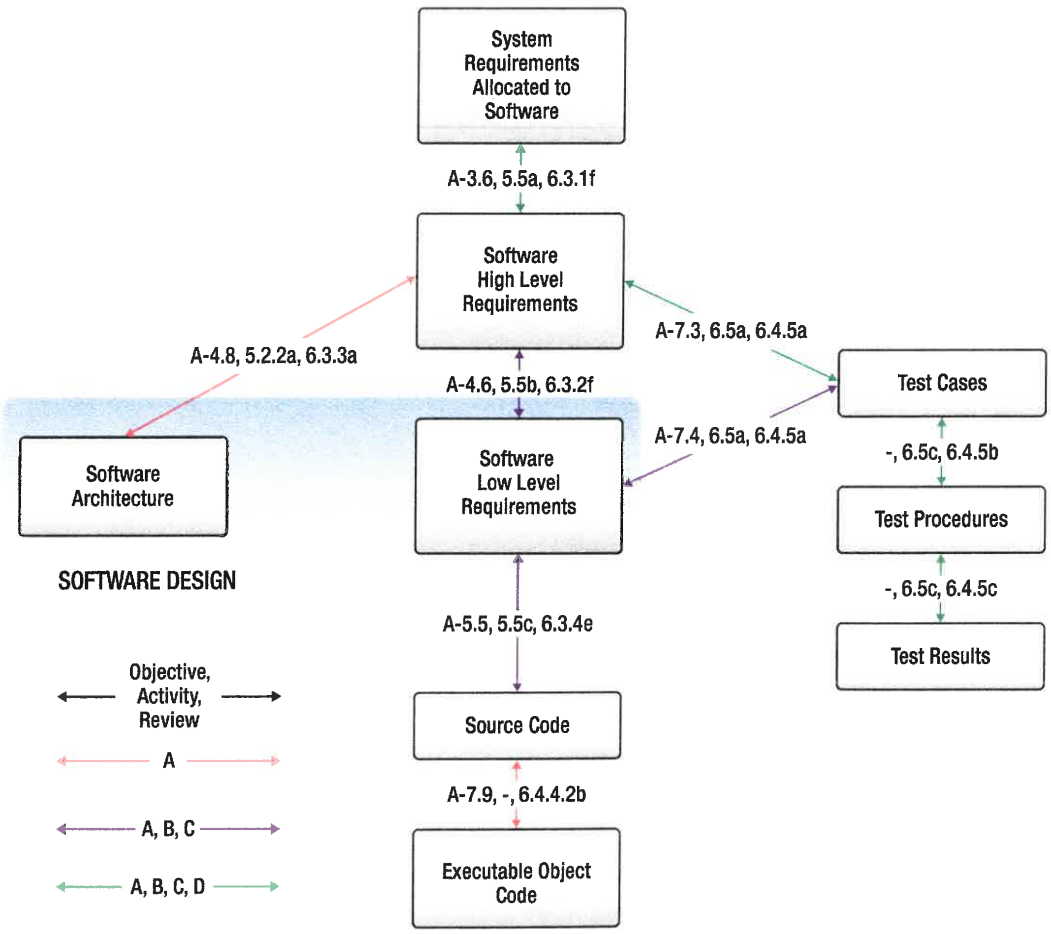


Figure 13-1. DO-178C required traceability between software artifacts.

Question: 13-1
Software management control includes a thorough definition and documentation of the aircraft software development process. What documentation is required?

Question: 13-2
What is DO-178 and why is it important?

Question: 13-3
Why are flight control and navigation systems certified at DO-178 Level A?

Question: 13-4
What is ARINC 653 and where is it used?

Question: 13-5
What was DO-178C developed to take the place of DO-178B?

Question: 13-6
DO-178C requires tracing between which certification artifacts for Level A software applications that are not required for any other levels?

ANSWERS

Answer: 13-1
Documentation includes: airworthiness certification plan, software quality assurance plan, software configuration management plan, configuration control procedures, software code standard, software design standard, software requirements standard, software development plan, software verification plan, software design document, software requirements document, traceability, test cases and test procedures, verification results, quality assurance records, configuration management records, problem reports, and a software accomplishments summary.

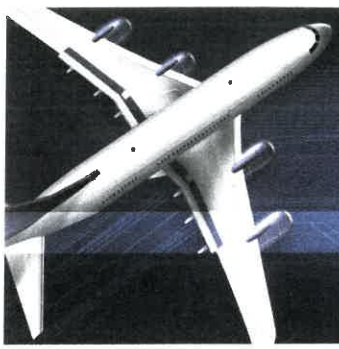
Answer: 13-2
DO-178 is a standards document dealing with the safety of software used in aircraft systems. DO-178 established design assurance levels based on a safety assessment process and hazard analysis by examining the effects of a failure condition in each aircraft system. The Federal Aviation Administration (FAA) and European Aviation Safety Agency (EASA) have used DO-178 as certification guidance to determine if the software will perform reliably in aircraft systems.

Answer: 13-3
Flight control and navigation systems are flight critical, and thus require Level A certification, because failure may cause multiple fatalities and loss of aircraft.

Answer: 13-4
ARINC 653 is a software specification for space and time partitioning in a real-time operating system that allows a processor to host multiple software applications of different criticality levels on the same processor. ARINC 653 is used in Integrated Modular Avionic (IMA) systems to isolate flight-critical functions from non-flight-critical functions so that if a software application fails, it can't take down the entire IMA system.

Answer: 13-5
When DO-178B was initially published, most software was coded by hand. However, software development processes have since evolved to automatic coding using model-based design. As such, there was a need for clarification or refinement of the definitions between high-level system requirements and low-level software requirements. Also required was a process to determine how to verify software that was model-based and determine if model-based simulation or formal methods could replace some or all of the software testing activities.

Answer: 13-6
DO-178C Level A requires traceability between the source code and executable object code be documented.



DIGITAL TECHNIQUES ELECTRONIC INSTRUMENT SYSTEMS

ELECTROMAGNETIC ENVIRONMENT

SUB-MODULE 14

PART-66 SYLLABUS LEVELS

CERTIFICATION CATEGORY → B2

Sub-Module 14

ELECTROMAGNETIC ENVIRONMENT

Knowledge Requirements

5.14 - Electromagnetic Environment

Influence of the following phenomena on maintenance practices for electronic system:	2
EMC-Electromagnetic Compatibility	
EMI-Electromagnetic Interference	
HIRF-High Intensity Radiated Field	
Lightning/lightning protection	

5.14 - ELECTROMAGNETIC ENVIRONMENT

Unintended electromagnetic waves can cause severe disruption to aircraft system operation. Electromagnetic waves have both an electric and magnetic component. As discussed in *Sub-Module 12*, static electric charges set up an influence around them, which is described as an electric field. At each point in space, electric field strength can be measured in terms of volts per meter. Electrostatic induction occurs when a charged object induces the redistribution of charges in another object, such as the example of picking up pieces of paper using a comb that was rubbed against fur due to the attraction of opposite charges.

However, when electrons are moving through a conductor producing an electric current, an additional influence occurs, which is described as a magnetic field. Magnetic field strength is measured in amperes per meter. As shown in ***Figure 14-1***, the magnetic field radiates at a right angle to the electrical current traveling through the conductor. The direction of the magnetic lines of force will travel counter-clockwise if the current if flowing towards the viewer. This is called the "right-hand grip" rule because if the viewer grips the wire with the right hand and the thumb is pointed in the direction of the current, the fingers would wrap around the wire in a direction indicating the motion of the magnetic lines of force, called flux.

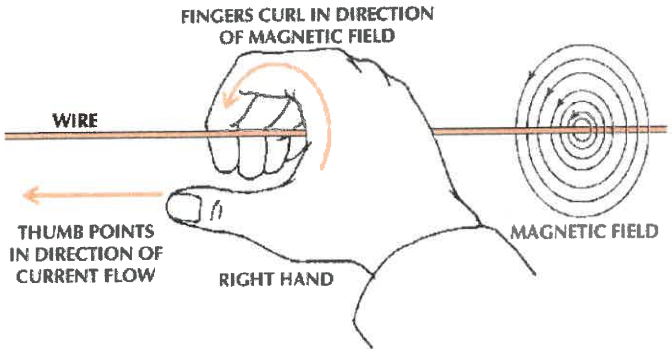


Figure 14-1. Magnetic flux field radiates at a right angle to direction of electrical current.

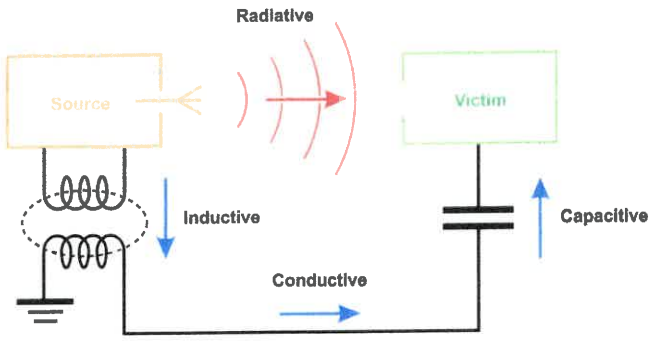


Figure 14-2. The four known emi coupling methods.

ELECTROMAGNETIC INTERFERENCE (EMI)

As shown in ***Figure 14-2***, there are four ways that electromagnetic fields can be coupled between the source of the unintentional generation of electromagnetic energy and the victim that suffers from its unwanted effects. These four EMI coupling methods can work together or independently, providing either continuous or transient (electromagnetic pulse) interference.

Electromagnetic fields, in the frequency range from DC to light, constantly radiate in to space. For example, a transmitter antenna radiates electromagnetic RF waves to a receiver antenna. Radiative coupling occurs when the source emits or radiates an electromagnetic field that propagates across an open space and is received by the unintended victim. Inductive coupling and capacitive coupling occur over much shorter distances than radiative coupling. Inductive coupling occurs when a varying magnetic flux field from one conductor comes in close proximity to another conductor producing an induced current. Capacitive coupling occurs when a varying electric field exists between two adjacent conductors inducing a voltage change between the conductors through a dielectric, such as air. Finally, conductive coupling occurs when the coupling path between the source and the victim is formed by direct contact through perhaps a wire or metal enclosure.

HIGH-INTENSITY RADIATED FIELD (HIRF)

Of particular concern to aviation safety authorities is the presence of High-Intensity Radiated Fields (HIRF) whereby the power density of the electromagnetic field is sufficient to adversely affect living organisms or degrade equipment performance. A common HIRF device found in aircraft galleys is a microwave oven. Food and beverage items placed in the oven are heated through electromagnetic radiation. HIRF interference can also be caused by high power radio and microware towers,

including ATC primary surveillance radars. Evidence has revealed that most of the crashes of the U.S. Army's UH-60 Black Hawk helicopter in the 1980's was caused by a malfunction in the electronic flight control system that was highly susceptible to the High-Intensity Radiated Fields from radio broadcast tower emissions.

Radio frequencies are radiated from the aircraft either deliberately or accidently. Aircraft communications, surveillance and radar equipment radiate RF waves from 10 MHz to tens of GHz. Care must be taken to prevent mutual HIRF interference between transmitters of one system and receivers of another system. Also, accidental radiation can occur when equipment is malfunctioning or wiring is incorrectly installed without proper grounding. Such radiation can cause corruption of bus data by inducing bit errors in the digital data stream.

LIGHTNING/LIGHTNING PROTECTION

Lightning is one of the most energetic of all electromagnetic phenomena. Prior to a lightning discharge, the potential difference between the earth and thunderclouds is approximately 100 million volts. Lighting strike measurements on aircraft indicate electric field strengths in the order of 50 kilovolts per meter and magnetic field strengths of up to 600 amperes per meter. Significant damage can occur to sensitive electronic equipment due to a high electromagnetic pulse (EMP) caused by a lightning strike.

Most aircraft are designed to operate in all weather conditions, and since it may not be possible to divert a flight to avoid a thunderstorm, aircraft are typically designed with both lightning detection and lightening protection capabilities. Since lightning emits a unique electromagnetic signal, it is a reliable means for identifying potentially dangerous weather for the flight crew to avoid. The azimuth of a lightning discharge can be calculated by an ADF receiver using a loop antenna. The field strength intensity (power density) of the lightning strike can reveal the distance from the thunderstorm. This information is typically displayed as symbology that is overlaid on the Weather Radar page on the Multifunction Display. (***Figure 14-3***)

For lighting protection, aircraft have static wicks installed at the trailing edge of the horizontal and vertical surfaces to dissipate electromagnetic energy on the surface of the skin back into the atmosphere. (***Figure 14-4***) An aluminum airplane is quite conductive and is able to dissipate the high currents resulting from a lightning strike. However, the use of composite materials in modern airliners, such as the Boeing 787 Dreamliner, with a fuselage made predominantly of carbon fiber, has required additional design features, such as putting some metal back into the fuselage for lightning protection.

Carbon fibers are 1 000 times more resistive than aluminum to current flow, and epoxy resin is 1 000 000 times more resistive. Therefore, the surface of an external composite component often consists of a ply or layer of conductive material for lightning strike protection because composite materials are less conductive than aluminum. Many different types of conductive materials

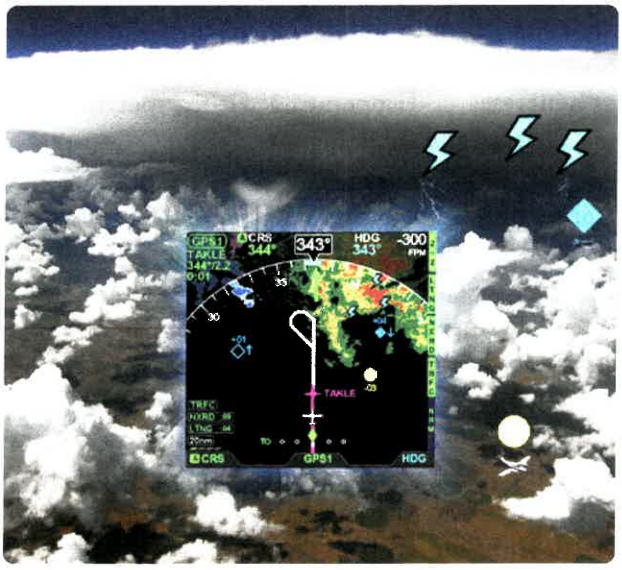


Figure 14-3. Lightning detection overlaid on a MFD weather radar page.

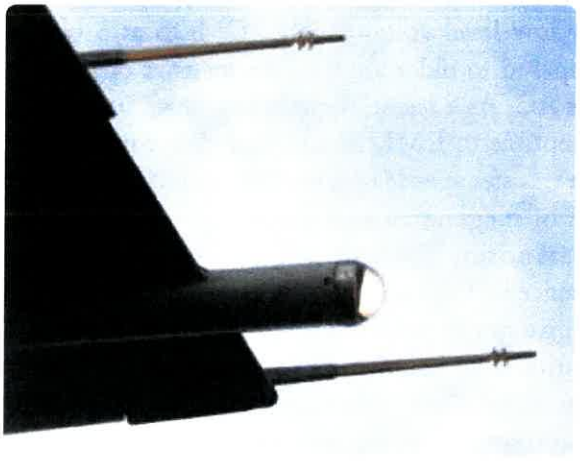


Figure 14-4. Static wicks on Boeing 737 wing.

are used ranging from nickel-coated graphite cloth to metal meshes to aluminized fiberglass to conductive paints. In addition to a normal structural repair, the technician must also recreate the electrical conductivity designed into the part. All components must be electrically bonded to one other with a metal-braided bonding strap to ensure conductivity across the entire aircraft structure. These types of repair generally require a conductivity test to be performed with an ohmmeter to verify minimum electrical resistance across the structure.

ELECTROMAGNETIC COMPATIBILITY (EMC)

The goal of Electromagnetic Compatibility is to eliminate or reduce the harmful effects of unintended Electromagnetic Interference. EMC is achieved by addressing both emission and susceptibility issues, i.e., quieting the sources of interference and hardening the potential victims from attack. In terms of emission, EMC is concerned with keeping electrical equipment that generates EMI operating within specified limits using filtering and shielding.

In terms of susceptibility, EMC addresses the design and operation of equipment that makes it immune to small levels of EMI that can't be entirely eliminated. As such, requirements are placed on equipment and wiring installation that involves the separation of wiring bundles and equipment including signal wire segregation. It also requires proper screening and bonding of equipment racks and RF sealing of equipment. These steps will help obviate the effects of EMI, HIRF, and lightning strikes on or near the aircraft.

EMC has become ever more important since the introduction of digital electronics, which operate on very low-level voltages (e.g., CMOS at 3 volts DC) compared to older analog systems that operate at 115 volts AC. As a result, digital electronics are much more susceptible to EMI. In addition, faster processing and data transfer speeds require higher clock rates of several tens of megahertz and much shorter pulse rise and fall transition times of only a few nanoseconds. The presence of fast pulses on PCBs and data bus transfers can give rise to radiation coupling (crosstalk) to adjacent circuits. The problem is exacerbated with the trend of modern aircraft being manufactured mostly out of light-weight composite carbon graphite materials that lack the electromagnetic shielding provided by aluminum structures. Therefore, it is the responsibility of the aircraft technician to ascertain the nature and significance of electromagnetic emissions from all equipment and the effects of any externally generated interference on the operation of all aircraft systems. EMI should be identified and eliminated, or at least reduced as much as possible at the source by eliminating coupling paths through proper equipment layout, shielding, filtering, and grounding techniques.

In accordance with MIL-STD-461, LRUs should be designed with EMI sensitive electronics located on one side of the enclosure, forming a 'Faraday cage' that is shielded from EMI effects so that sensitive microelectronic devices can be operated in a protected environment. All signals entering the EMI 'clean' area should be filtered to remove voltage spikes and surges. The EMI 'dirty' components, such as the power supply unit, that radiate EMI and can withstand to operate in this environment, should be isolated on the other side of the enclosure away from the shielded 'clean' compartment. When an LRU is opened for maintenance, it is imperative that it is reassembled correctly with all shielding and grounding mechanisms put back in place. (***Figure 14-5***)

Finally, cabling should be shielded and grounded to protect the wiring from external radiated interference from passenger electronic devices, such as laptop computers and cellular phones, and from HIRF and lightning strikes. Ultimately, it is the responsibility of the highly qualified aircraft technician to assure that EMI is contained by performing proper maintenance procedures to assure EMC functional integrity of all aircraft systems.

Figure 14-5. Heat-sink shield acts as a faraday cage to block electromagnetic emissions.

Question: 14-1
Explain the "right-hand grip" rule for current flowing through a conductor.

Question: 14-2
What are the four methods of electro-magnetic coupling?

Question: 14-3
What are High-Intensity Radiated Fields (HIRF) and why are they of concern?

Question: 14-4
How is lightning detected for identifying potentially dangerous weather for the flight crew to avoid?

Question: 14-5
How must carbon composite aircraft structures be repaired to protect the aircraft from the adverse effects of lightning strikes?

Question: 14-6
What is the responsibility of the technician when it comes to Electromagnetic Compatibility (EMC)?

ANSWERS

Answer: 14-1
The magnetic field radiates at a right angle to the electrical current traveling through a conductor. The direction of the magnetic lines of force (flux) will travel counter-clockwise if the current if flowing towards the viewer. This is called the "right-hand grip" rule because if the viewer grips the wire with the right hand and the thumb is pointed in the direction of the current, the fingers would wrap around the wire in a direction indicating the motion of the magnetic lines of force.

Answer: 14-2
Radiative coupling occurs when the source emits or radiates an electromagnetic field that propagates across an open space and is received by the unintended victim. Inductive coupling occurs when a varying magnetic flux field from one conductor comes in close proximity to another conductor producing an induced current. Capacitive coupling occurs when a varying electric field exists between two adjacent conductors inducing a voltage change between the conductors through a dielectric, such as air. Finally, conductive coupling occurs when the coupling path between the source and the victim is formed by direct contact.

Answer: 14-3
Of particular concern to aviation safety authorities is the presence of HIRF whereby the power density of the electromagnetic field is sufficient to adversely affect living organisms or degrade equipment performance. HIRF interference caused by radio and microware towers have been shown to cause malfunctions in the electronic flight control systems leading to aircraft incidents causing loss of life.

Answer: 14-4
The azimuth of a lightning discharge can be calculated by an Automatic Direction Finder (ADF) receiver using a loop antenna. The field strength intensity (power density) of the lightning strike can reveal the distance from the thunderstorm. This information is typically displayed as symbology that is overlaid on the Weather Radar page on the Multifunction Display.

Answer: 14-5
In addition to a normal structural repair, the technician must recreate the electrical conductivity designed into the part. All components must be electrically bonded to one other with a metal-braided bonding strap to ensure conductivity across the entire aircraft structure. These types of repair generally require a conductivity test to be performed with an ohmmeter to verify minimum electrical resistance across the structure.

Answer: 14-6
Accidental radiation can occur when equipment is malfunctioning or wiring is incorrectly installed without proper grounding. Such radiation can cause corruption of bus data by inducing bit errors in the digital data stream. As such, requirements are placed on equipment and wiring installation that involves the separation of wiring bundles and equipment including signal wire segregation. It also requires proper screening and bonding of equipment racks and RF sealing of equipment.

DIGITAL TECHNIQUES ELECTRONIC INSTRUMENT SYSTEMS

TYPICAL ELECTRONIC/DIGITAL AIRCRAFT SYSTEMS

SUB-MODULE 15

PART-66 SYLLABUS LEVELS

CERTIFICATION CATEGORY → B2

Sub-Module 15

TYPICAL ELECTRONIC/DIGITAL AIRCRAFT SYSTEMS

Knowledge Requirements

5.15 - Typical Electronic/Digital Aircraft Systems

General arrangement of typical electronic/digital aircraft systems and associated BITE (Built In Test Equipment) such as: 2

(a) For B1 and B2 only:
ACARS-ARINC Communication and Addressing and Reporting System
EICAS-Engine Indication and Crew Alerting System
FBW-Fly by Wire
FMS-Flight Management System
IRS-Inertial Reference System

(b) For B1, B2 and B3:
ECAM-Electronic Centralised Aircraft Monitoring
EFIS-Electronic Flight Instrument System
GPS-Global Positioning System
TCAS-Traffic Alert Collision Avoidance System
Integrated Modular Avionics
Cabin Systems
Information Systems

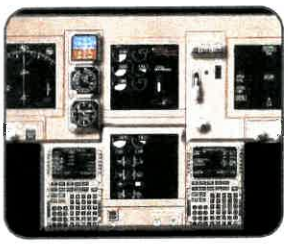
5.15 - DIGITAL AIRCRAFT SYSTEMS

The first Sub-Module discussed Electronic Instrument Systems (EIS). Subsequent Sub-Modules discussed digital electronics for aircraft applications in general. As shown in ***Figure 15-1***, this final Sub-Module will expand on that discussion to include Integrated Modular Avionics Information Systems used to control onboard communications, navigation and surveillance systems and to provide information to be displayed on the EIS. It will also discuss how the crew uses this information to command the Flight Control System to fly the aircraft at the desired altitude, attitude, direction and airspeed. Finally, this Sub-Module will conclude with a discussion on cabin electronic systems.

As shown in ***Figure 15-2***, most of the electronics in the Boeing 777 reside in the main equipment center racks located under the cockpit floor and above the nose gear wheel well. The flight control electronics and air data/ inertial reference unit are located on the bottom two shelves of the E1 and E2 racks. The cabin electronics are situated immediately above that in the third shelf from the bottom. The second and third shelves from the top are where the following Communication, Navigation and Surveillance (CNS) LRUs are located:

- Communications – Very-High Frequency (VHF) Communications Transceivers and the SELCAL (SELective CALling) unit. (Note: The High-Frequency (HF) Communication and Satellite Communication (SATCOM) transceivers used for long-distance and over-the-ocean communications are located further aft in the fuselage.)
- Navigation – Automatic Direction Finder (ADF), Instrument Landing System (ILS), VHF Omni-Range (VOR), Distance Measuring Equipment (DME) and Marker Beacon.
- Surveillance - Air Traffic Control (ATC) Transponders and Traffic Alert and Collision Avoidance System (TCAS).

The top shelf on the E2 rack contains one of two of the Airplane Information Management System (AIMS) cabinets. The second AIMS cabinet is located in the E3 rack directly opposite the E2 rack looking forward. AIMS contains the electronics for the Electronic Instrument System and Flight Management System, in addition to the Communications Management System, which controls the Aircraft Communication Addressing and Reporting System (ACARS).



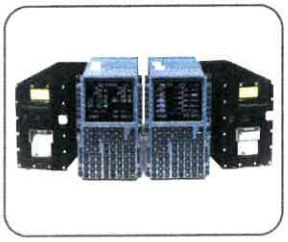
ELECTRONIC INSTRUMENT SYSTEM (EIS)

Electronic Flight Instrumentation System (EFIS)

Engine Indication and Crew Alerting System (EICAS)

Electronic Centralized Aircraft Monitor (ECAM)

Integrated Modular Avionics (IMA) Information Systems



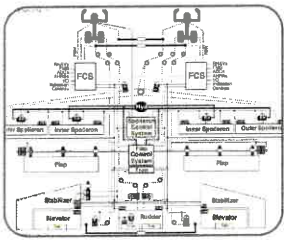
COMMUNICATIONS, NAVIGATION AND SURVEILLANCE (CNS) SYSTEM

Aircraft Communication Addressing and Reporting System (ACARS)

Flight Management System (FMS)

Inertial Navigation System (INS) and Global Positioning System (GPS)

Traffic Collision Avoidance System (TCAS)



FLY-BY-WIRE FLIGHT CONTROL SYSTEM (FCS)

Flight Deck Controls

Flight Director System

Autopilot and Actuators

Figure 15-1. Typical electronic/digital aircraft systems.

EQUIPMENT CENTERS

Main Equipment Center Racks

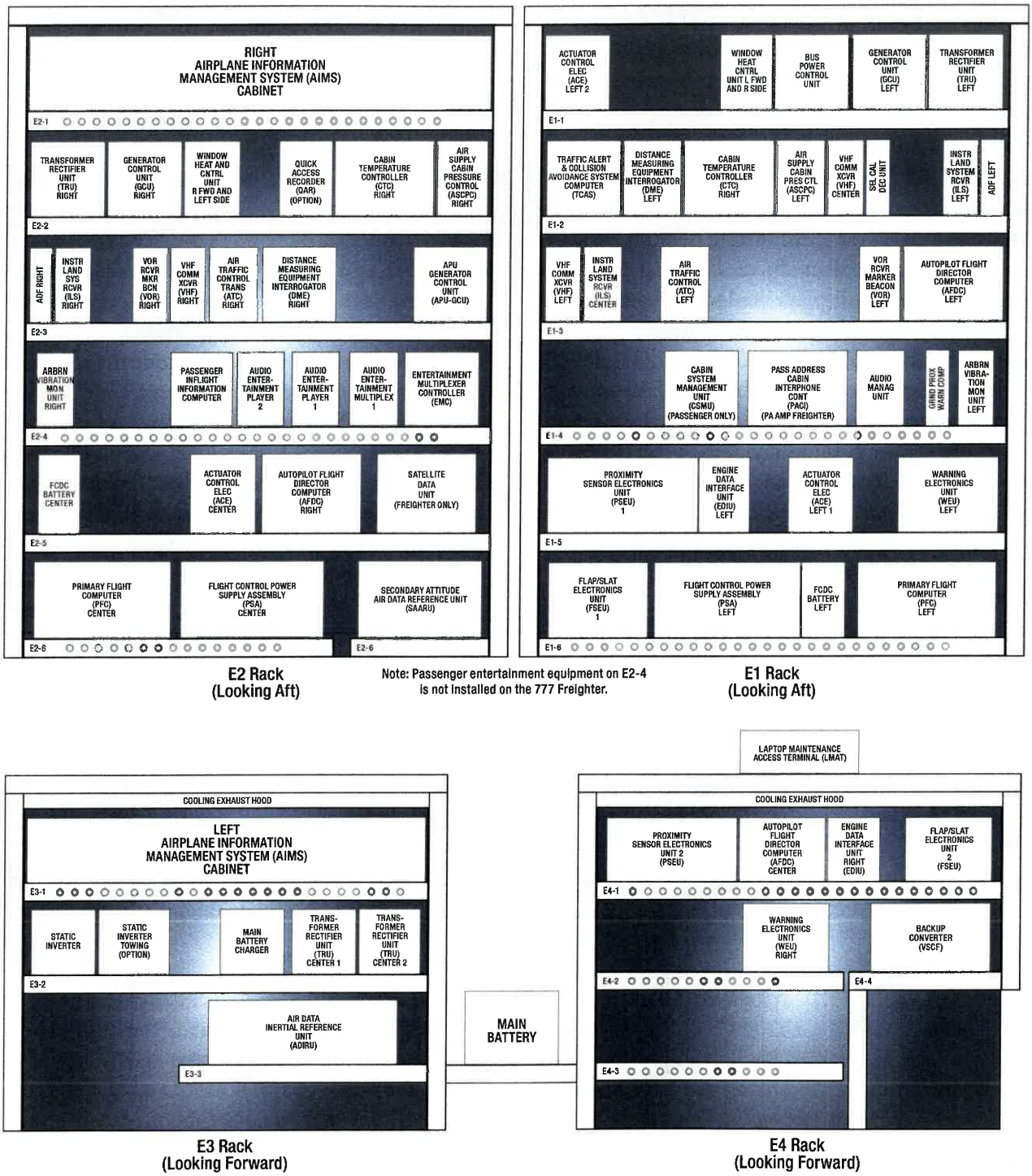


Figure 15-2. Boeing 777 main equipment center racks.

ELECTRONIC INSTRUMENT SYSTEMS

ELECTRONIC FLIGHT AND ENGINE INSTRUMENTS

As previously discussed, the Boeing 777 EIS consists of a dual-redundant Electronic Flight Instrument Systems (EFIS) and Engine Indication and Crew Alerting System (EICAS). On the left side of the instrument panel is the Captain's EFIS, consisting of a Primary Flight Display (PFD) and a Navigation Display (ND). The Co-Pilot's EFIS has an identical PFD and ND. Boeing's Engine Indication and Crew Alerting System, also known as an Electronic Centralized Aircraft Monitor (ECAM) on Airbus aircraft, monitors the aircraft systems. Two EICAS displays are located in the center instrument panel. The lower EICAS display is known as a Multi-Function Display (MFD). ***Figure 15-3*** is a schematic diagram of the Boeing 777 EIS showing the display processing being performed by the Airplane Information Management System, which will be discussed in more detail in the following paragraphs.

INTEGRATED MODULAR AVIONICS (IMA), INFORMATION SYSTEMS, AND BITE

The avionic system architectures that became well established in the mid-1970's are still the standard architectures of current aircraft in service today. These are referred to as "federated architectures" because each LRU contains its own independent dedicated function, such as the CNS LRUs discussed previously. The federated box concept worked well for many years because there were well defined functional boundaries between LRUs, thereby providing a clear division of areas of responsibility between the various avionics suppliers. However, the disadvantage of the federated approach was that there was a duplication of processors, memories, and power supplies making the overall system much heavier and costly than it needed to be. With the recent advance of digital electronics, it became possible to combine these independent software (SW) functions into a singular cabinet of Line Replaceable Modules (LRMs). (***Figure 15-4***)

The IMA (Integrated Modular Avionics) concept provides a more unified approach to avionics design resulting in considerable less volume and weight due

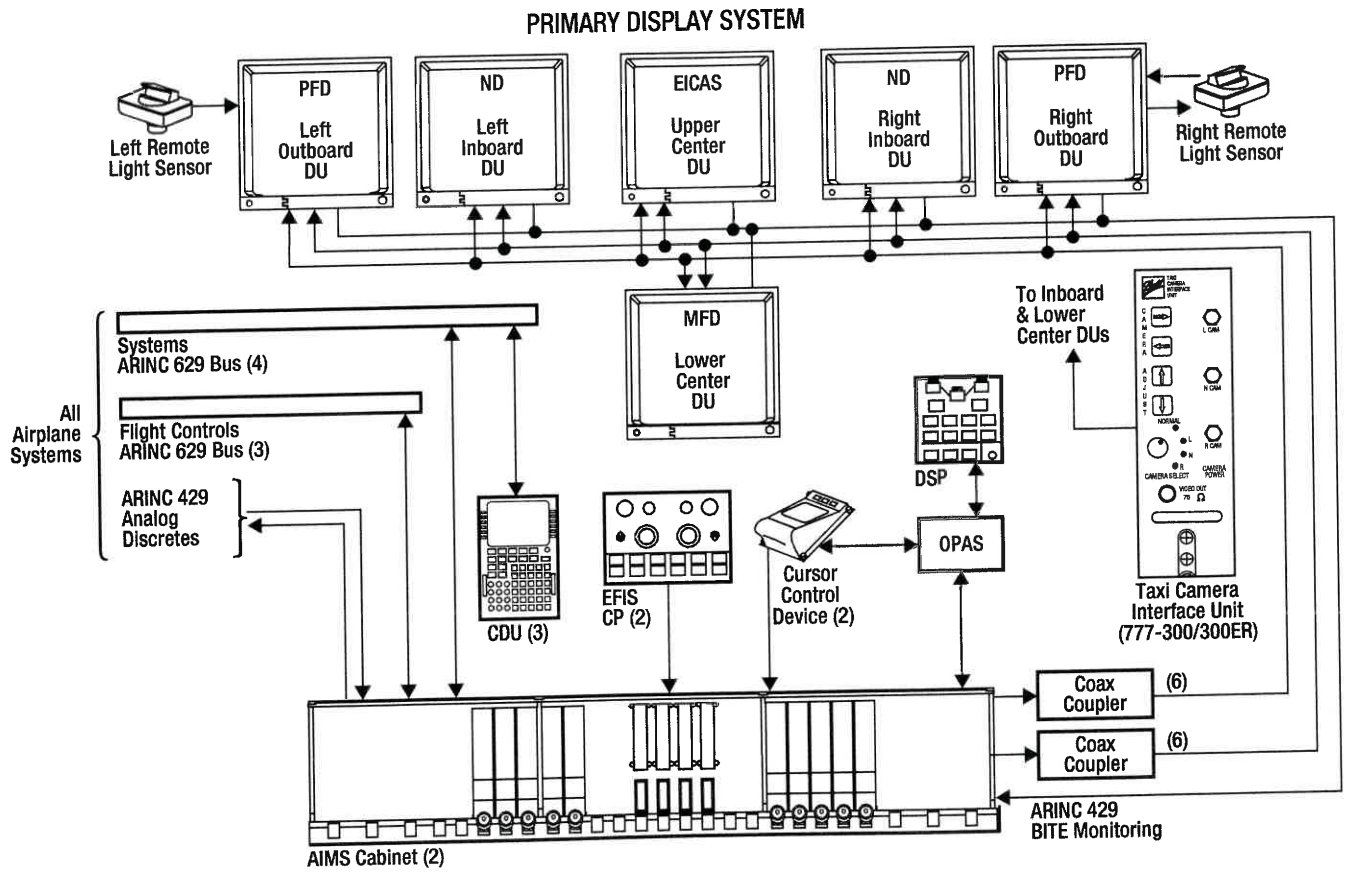


Figure 15-3. Boeing 777 electronic instrument system schematic diagram.

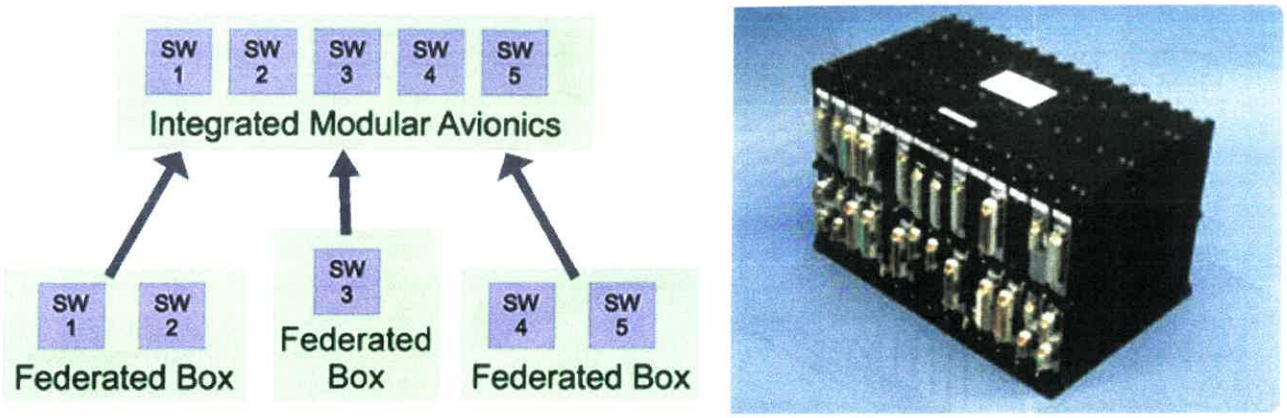


Figure 15-4. IMA Concept (left) and a typical IMA Cabinet (right).

to the sharing of resources across a number of Line Replaceable Modules. Many of the LRMs have identical hardware whose functionality differs only by the desired software application program installed. This commonality provides a pool of spare resources which improves system availability. In addition, high levels of fault detection and isolation are designed in the BITE (Built-In-Test Equipment) which allows for the replacement of a faulty module on the aircraft with the module being returned to the manufacturer for repair.

The only real disadvantage is that each of the avionic manufacturers must agree on a common set of form, fit and function standards in order that their LRMs fit in the cabinet and they function properly with other LRMs.

The Boeing 777, which first entered service in 1995, was the first commercial aircraft to make use of the Integrated Modular Avionics concept in what Boeing calls its Airplane Information Management System (AIMS), the main computer for many avionic systems. AIMS integrates multiple functions that require large quantities of data collection and processing. (***Figure 15-5***)

It consists of two cabinets with each cabinet containing 10 LRMs: 2 Core Processor Modules (CPMs) with bus communications capability, 2 CPMs with display graphic generators, 4 CPMs with I/O capabilities, and 2 power conditioning modules. In addition, ARINC 653 software partitioning allows the integration of multiple computing applications in a singular CPM and isolates flight-critical functions from mission-critical functions so that if a single software application fails, it can't take down the entire AIMS.

AIMS interfaces with approximately 130 LRUs, sensors, switches, and indicators to permit the integration of information from a majority of aircraft systems in one place. The onboard maintenance system uses AIMS for the BITE computing function. The maintenance crew uses a Maintenance Access Terminal (MAT) to control the central maintenance computing system and the airplane condition monitoring system. The MAT is a station with a display module, disk drive module, keyboard, and cursor control located at the observer station in the cockpit.

COMMUNICATIONS, NAVIGATION AND SURVEILLANCE SYSTEMS

AIRCRAFT COMMUNICATION ADDRESSING AND REPORTING SYSTEM (ACARS)

Airlines pay their flight and cabin crews based on the times reported for Out-of-the-gate, Off-the-ground, On-the-ground, and In-the-gate (OOOI). Prior to the introduction of data link to aircraft for sending text-based messages, the flight crew would verbally report their OOOI times to the Dispatch radio operators using their VHF or HF communication transceivers.

ACARS was originally called ARINC Communication Addressing and Reporting System because it was developed by ARINC in 1978 as a digital data link for transmission of short text messages between aircraft and ground stations to relieve the crew from having to call in their times and to provide more accurate reporting. The ARINC 597 standard defines the operation of the ACARS Management Unit, which uses discrete (on/off) inputs from the landing gear doors, parking brake and weight-on-wheels sensors to automatically determine the OOOI times and send these as text messages.

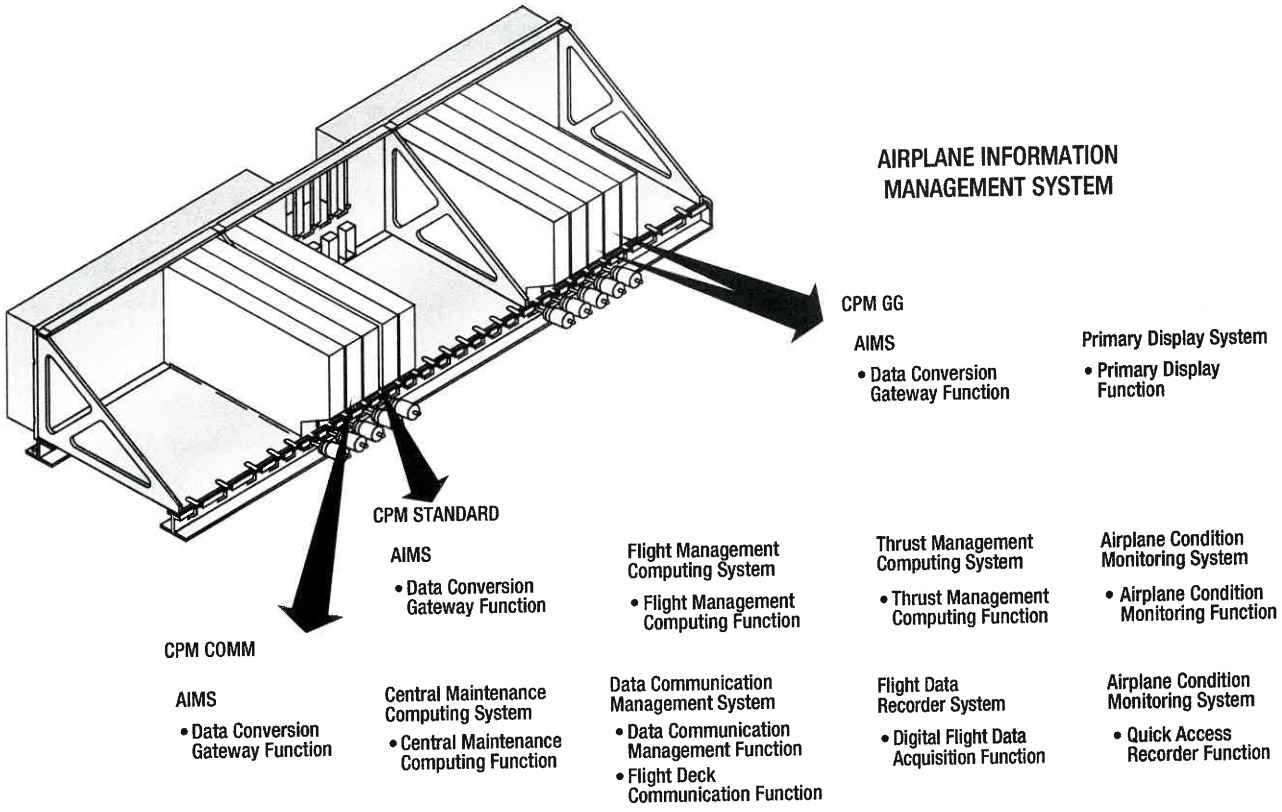


Figure 15-5. Airplane information management system cabinet.

ACARS also has a Medium Shift Keying modem that is used to transmit the OOOI reports over existing VHF or HF radios.

Figure 15-6 shows a typical ACARS display format prior to landing. As the plane comes out of cruise altitude, ACARS begins updating the Dispatch office with a new estimated time of arrival and other changing details so that appropriate preparations, such as gate assignment and barrage handling, can be made. On touchdown, the ACARS report is automatically sent to Dispatch and the next crew heads for the gate. When the airplane comes to a final stop, the entire report is sent to a printer. The Captain signs the report securing the crew's pay for the day.

Figure 15-6. Typical ACARS display format.

INERTIAL NAVIGATION SYSTEM (INS)

Traditional radio navigational aids, such as VOR and DME, require external ground-based references to provide a navigation solution. However, Inertial Navigation Systems, also known as Inertial Reference Systems (IRS), are self-contained navigation aids that use rotation sensors, motion sensors and a computer to continuously calculate (via dead reckoning) the position, orientation, and velocity of the aircraft without the need for external references. This is essential for over-water navigation where no ground-based navigation sensors exist.

Inertial navigation uses gyroscopes to measure angular velocity, and acceleration meters to measure linear acceleration. Gyros and accelerometers are placed on each of the three axis (pitch, roll and yaw) on a gimbal assembly, commonly referred to as a stabilized platform. (***Figure 15-7 Left***) The flight crew enters an initial

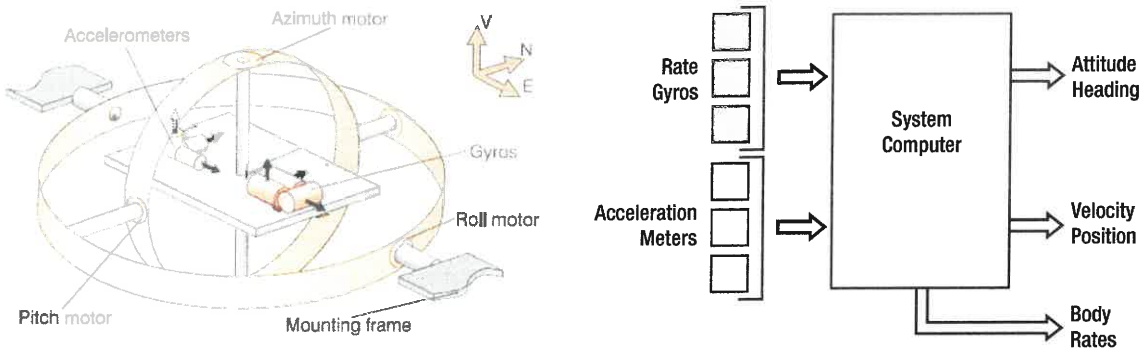


Figure 15-7. Gyro-stabilized IMU (left) and Strapdown IMU (right).

geographic position (latitude and longitude) on the ground prior to takeoff, and while in flight, the Inertial Measuring Unit (IMU) detects a change in geographic position, velocity (speed and direction), and orientation (attitude and body rates) for a computer to process to provide the flight crew with a total navigation solution.

Modern aircraft today use Strapdown IMUs in place of a gyro-stabilized platforms that contain many unreliable precision moving parts. (***Figure 15-7 Right***) With a Strapdown IMU, the gyros and accelerometers for each axis are "strapped down" to the aircraft thereby eliminating the need for gimbals, bearings, or torque motors to stabilize the platform. Strapdown systems use rate gyros to measure the change in angular velocity in each axis. Digital computers make it possible to integrate the changes in pitch, roll and raw at a rate of 2 000 Hz providing extreme accuracy.

Ring Laser Gyros

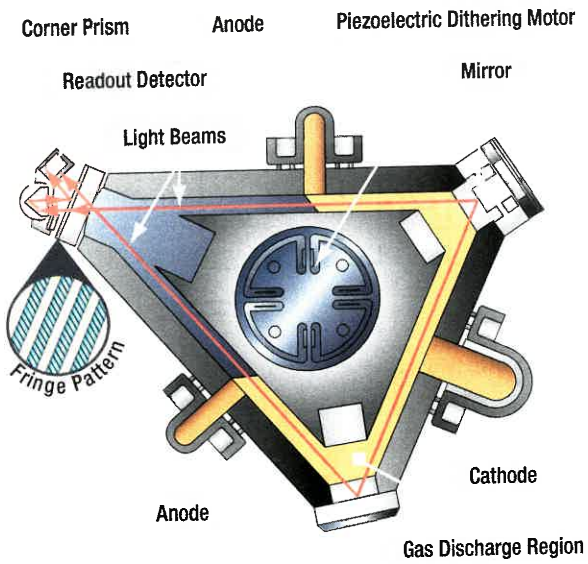
Most rate gyros are now laser interferometers, also called laser gyros. Laser gyros measure angular rate by employing the properties of two laser beams inside a triangular ring-shaped tuned cavity. The Ring-Laser Gyro (RLG) is made from a triangular block of glass with two tunnels drilled parallel to the perimeter of the triangle and with reflective mirrors placed in each corner. (***Figure 15-8 Top***)

A small charge of helium and neon gas is inserted and the cavity is sealed. When high voltage is applied between the anodes and cathode, the gas becomes ionized and forms two high energy light beams (lasers) that travel around the cavity in opposite directions. Since both counter-rotating beams travel at the constant speed of light, it takes each beam the exact same time to complete its triangular path. However, if the gyro was rotated on its axis, the path of one beam would be shortened, while the path for the other beam would be lengthened. This is known as the Sagnac effect. (***Figure 15-8 Bottom***) In addition, the laser beam adjusts its wavelength, and hence its frequency, for the length of the path. Since wavelength and frequency are inversely proportional, the laser beam that traveled the shorter distance would increase in frequency, and the laser beam that traveled the further distance would decrease in frequency. This frequency difference, as measured by the photocell detectors at one end of the triangle, is directly proportional to angular rate of turn about the gyro's axis.

Micro-Electro Mechanical System (MEMS)

The latest technology used for inertial reference are solid-state Micro-Electro-Mechanical System (MEMS) devices. Through the use of solid-state MEMS devices, reliability is increased while weight and volume is decreased, primarily due again to the lack of moving parts. Tiny vibrating piezoelectric IMUs with resistance and capacitance pick-offs are accurate and reliable and only a few millimeters in length and width. They are normally integrated into an Integrated Circuit chip designed to yield an output after various conditioning processes are performed. The chips can be packaged for installation inside a dedicated computer LRU or LRM.

Regardless of which type of IMU device is employed, the advantage of having a self-contained navigation system is negated by the fact that all inertial systems have a tendency to drift, sometimes as much as 0.6 nautical miles per hour. Small errors in acceleration and angular rate measurements propagate in time into progressively larger errors in velocity and position. This is known as integration drift. Therefore, the inertial position must be periodically corrected by input from some other form of navigation system, such as DME or



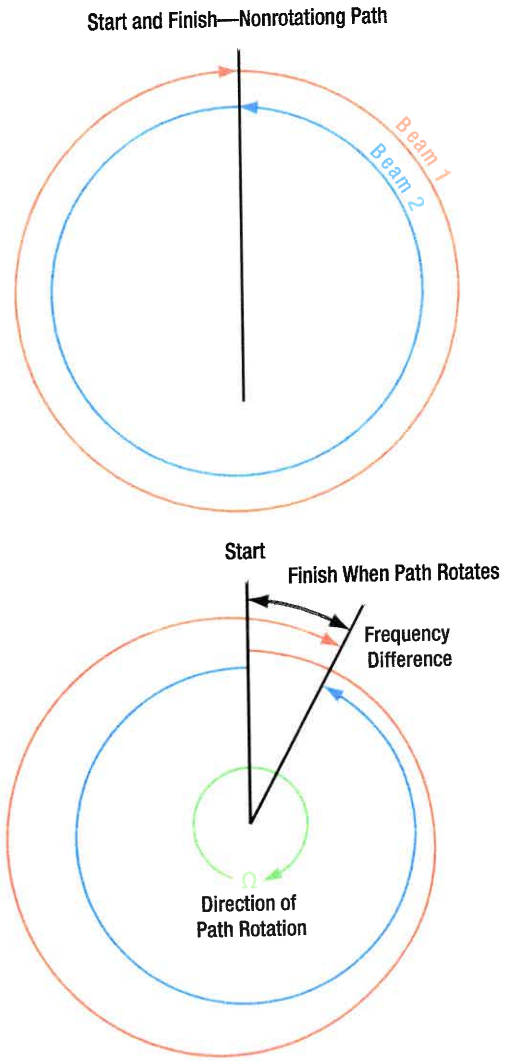


Figure 15-8. Sagnac Effect (bottom), Modern Ring-Laser Gyro IMU (top).

Global Positioning System. Since DME is a land-based navigation aid, GPS must be used to update the INS when flying over large bodies of water.

GLOBAL POSITIONING SYSTEM (GPS)

The Global Positioning System is a space-based navigation system that was launched by the U.S. Department of Defense in the early 1990's, and has since become very popular commercially, not only for aircraft navigation, but for maritime, automotive and personal applications as well. It provides position data, velocity rate, and system time to GPS receivers all around the world.

GPS consists of three segments: a space system segment, a control system segment, and a user system segment. The space system segment consists of 6 planes of satellites, each plane containing 4 satellites, in precise 10 898 mile geostationary orbits. The control system segment has several monitoring stations located in U.S. controlled territory that track all satellites in view and accumulates ranging data to provide orbit determination and eliminate any errors. The user's GPS receiver computes its distance from the satellites by measuring the travel time of the satellite's signal. By using the distances from at least three satellites, the GPS receiver can triangulate the user's current position. With measurements from four satellites, the GPS receiver can determine elevation as well. (***Figure 15-9 Left***)

As previously stated, the INS measures acceleration and angular rates and mathematically integrates these into velocity and position. However, since the inertial system outputs are obtained through integration, they drift at a very low frequency. The GPS is an ideal reference for realigning and recalibrating the INS during flight.

As shown in ***Figure 15-9 Right***, an algorithm, known as a Kalman Filter, is used to provide error correction to the INS. In addition, the INS provides prepositioning data for re-acquiring the GPS signal should the signal be lost.

WIDE AREA AUGMENTATION SYSTEM (WAAS)

Unlike traditional ground-based navigation aids, the WAAS covers nearly all of the National Airspace System (NAS). The WAAS provides augmentation information to GPS receivers to enhance the accuracy and reliability of position estimates. The signals from

GPS satellites are received across the NAS at many widely-spaced Wide Area Reference Stations (WRS) sites. The WRS locations are precisely surveyed so that any errors in the received GPS signals can be detected. The GPS information collected by the WRS sites is forwarded to the WAAS Master Station (WMS) via a terrestrial communications network. At the WMS, the WAAS augmentation messages are generated. These messages contain information that allows GPS receivers to remove errors in the GPS signal, allowing for a significant increase in location accuracy and reliability. The augmentation messages are sent from the WMS to uplink stations to be transmitted to navigation payloads on geo-stationary communications satellites. (***Figure 15-10***)

The geo-satellite navigation transponders broadcast the augmentation messages on a GPS-like signal. The aircraft's GPS/WAAS receiver processes the WAAS augmentation message as part of estimating position. The GPS-like signal from the satellite navigation transponder can also be used by the receiver as an additional source for calculation of the user's position. WAAS also provides indications to GPS/WAAS receivers of where the GPS system is unusable due to system errors or other effects. Further, the WAAS system was designed to the strictest of safety standards – users are notified within six seconds of any issuance of hazardously misleading information that would cause an error in the GPS position estimate.

FLIGHT MANAGEMENT SYSTEM (FMS)

Flight Management Systems, which became popular in the mid-1980s, automates a wide variety of in-flight tasks previously performed by a human navigator; thereby, reducing the workload on the flight crew. Not only can it define a desired route from the aircraft's current position to any point in the world, but the route will be based on the aircraft's operating characteristics to manage overall flight performance.

On-time take-offs and landings, fuel conservation, and long engine and component life all contribute to airline profitability. The FMS helps achieve these results by operating the aircraft with much greater precision than humanly possible.

As shown in ***Figure 15-11***, the FMS consists of dual-redundant Flight Management Computers (FMC) and Control Display Units (CDU). During normal operation, the computers crosstalk with each other to share and compare information. Each FMC is capable of operating independently in the event the other FMC fails. However, only one FMC provides commands to the other aircraft systems at any one time.

Prior to take-off, the flight crew inputs their initial geographic location (latitude and longitude) and flight plans on one of the CDUs located in the center console. The FMC receives navigation and guidance information from the air data, inertial navigation, and global positioning system, in addition to ground-based radio navigational aids, and uses that information to compute ground speed, track, wind direction and velocity. The FMC then computes the optimum flight path, using a stored digital map terrain data base, to guide the aircraft to its final destination.

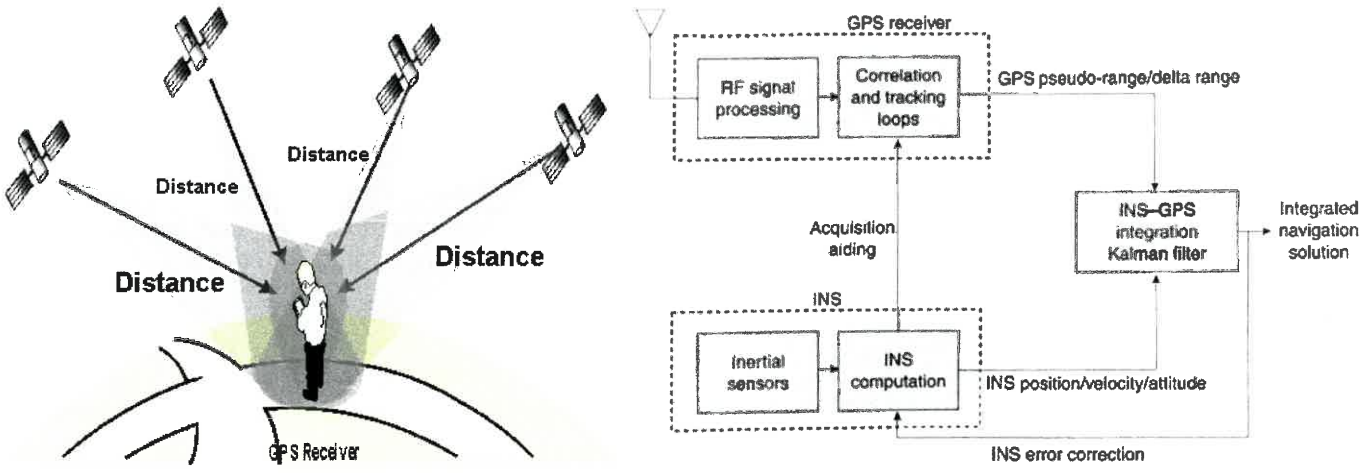


Figure 15-9. GPS Triangulation (left) and Integrated Navigation Solution (right).

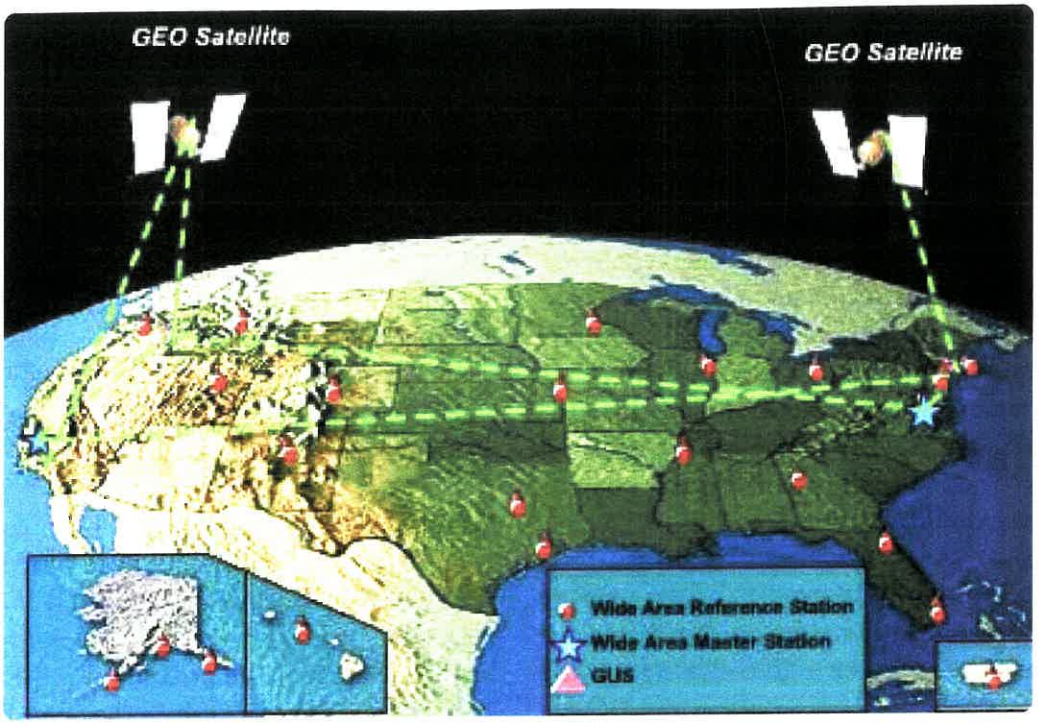


Figure 15-10. WMS generates augmentation messages for GPS error correction.

The FMC provides waypoints along the intended route on the EFIS Navigation Display (***Figure 1-8***) and drives the flight director steering command bars on the EFIS Primary Flight Display (***Figure 1-7***). The FMC communicates with the Thrust Management System (TMS) that drives the auto-throttle to control aircraft speed, and the automatic Flight Control System (FCS or AFCAS), that drives the actuators that move the control surfaces for lateral and vertical control along the computed flight path. The FMC continually optimizes the flight path as variables, such as wind speed and direction, change during flight.

Each flight path has vertical, horizontal, and navigational components, which are maintained by manipulating the engine and airframe controls. While doing so, numerous options are available to the pilot. Rate of climb, thrust settings, EPR (engine pressure ratio) levels, airspeed, descent rates, etc., can be varied. Commercial air carriers use the FMS to establish guidelines by which flights can be flown to promote the company's goals for fuel and equipment conservation. The flight crew need only enter variables as requested and respond to suggested alternatives as the FMS presents them. The FMS has stored in its database literally hundreds of flight plans with predetermined operational parameters that can be selected and implemented.

Integration with onboard radio navigational aids allows the FMC to change VOR, DME and ILS frequencies as the flight plan is enacted. Internal computations, using direct input from fuel flow and fuel quantity systems, allow the FMC to carry out lean operations or pursue other objectives, such as high performance operations if making up time is paramount on a particular flight. Weather and traffic considerations are also integrated. The FMC communicates to the crew via the CDU to present its planned action, gain consensus, or ask for an input or decision. The FMC continuously monitors its inputs for faults during operation. Maintenance personal can retrieve BITE generated information and pilot recorded fault messages. They may also access maintenance pages that identify faulty LRUs that have been identified by BITE.

TRAFFIC ALERT AND COLLISION AVOIDANCE SYSTEM (TCAS)

Traffic collision avoidance systems are transponder based air-to-air traffic monitoring and alerting systems. There are two classes of TCAS. TCAS I was developed to accommodate the general aviation community and regional airlines. This system identifies traffic in a 35 to 40 mile range of the aircraft and issues Traffic Advisories (TA) to assist pilots in visual acquisition of intruder aircraft. TCAS I is mandated on aircraft with 10 to 30 seats.

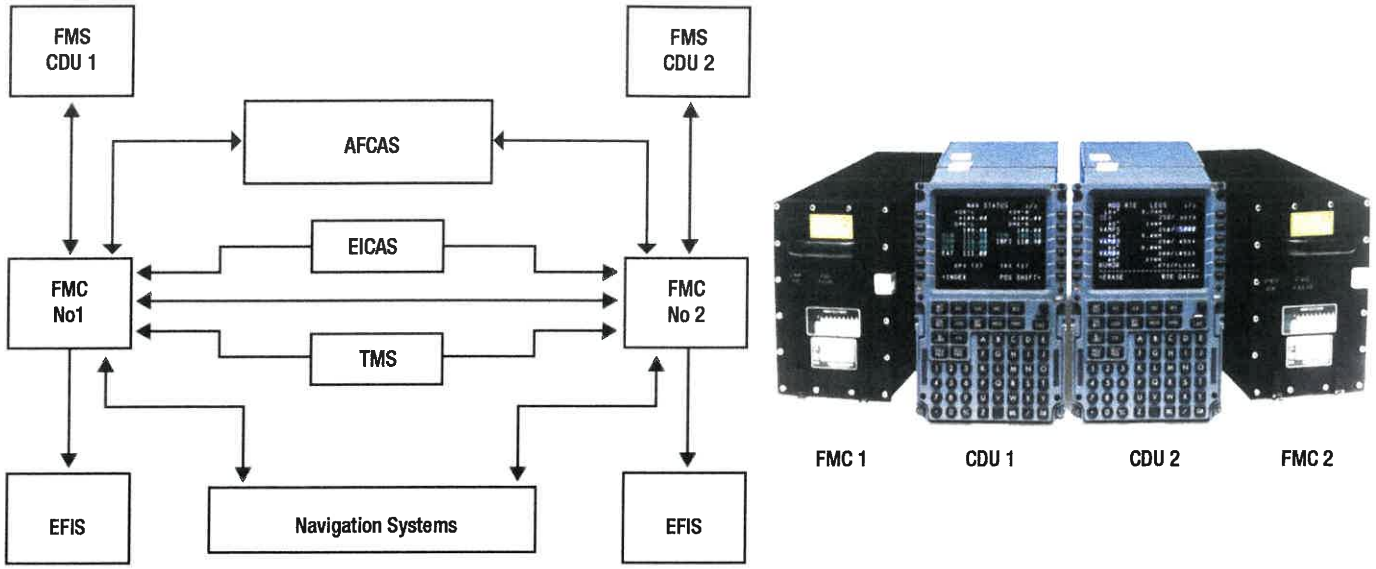


Figure 15-11. FMS Block Diagram (left) and FMS LRUs (right).

TCAS II is a more sophisticated system. It is required internationally in aircraft with more than 30 seats or weighing more than 15 000 kg. TCAS II provides the same information of TCAS I, but also analyzes the projected flight path of approaching aircraft. If a collision or near miss is imminent, the TCAS II computer issues a Resolution Advisory (RA). This is an aural and visual command to the pilot to take a specific evasive action. The computer is programmed such that the pilot in the encroaching aircraft receives an RA for evasive action in the opposite direction.

As shown in ***Figure 15-12***, TCAS issues an audible TA "TRAFFIC" alert when an intruder is 35-48 seconds away and issues an audible RA "CLIMB" or "DIVE" when an intruder is 20-30 seconds away. If vertical separation degrades to 850 feet, a TA warning appears, and at 600 feet, an RA command is issued both aurally and visually to both aircraft to take evasive action. An open diamond indicates a target; a solid diamond represents a target that is within 6 nautical miles or 1 200 feet vertically. A yellow circle represents a target that generates a TA. A red square indicates a target that generates an RA. A plus sign indicates the target aircraft is above and a minus sign indicates that it is below. The arrows show if the target is climbing or descending.

As shown in ***Figure 15-13***, the Transponder (XPDR) of an aircraft equipped with TCAS is able to interrogate the Transponders of other aircraft nearby using Secondary Surveillance Radar (SSR) Modes C and S. This is done with a 1030 MHz signal. Interrogated aircraft transponders reply with an encoded 1090 MHz signal that allows the TCAS computer to display the

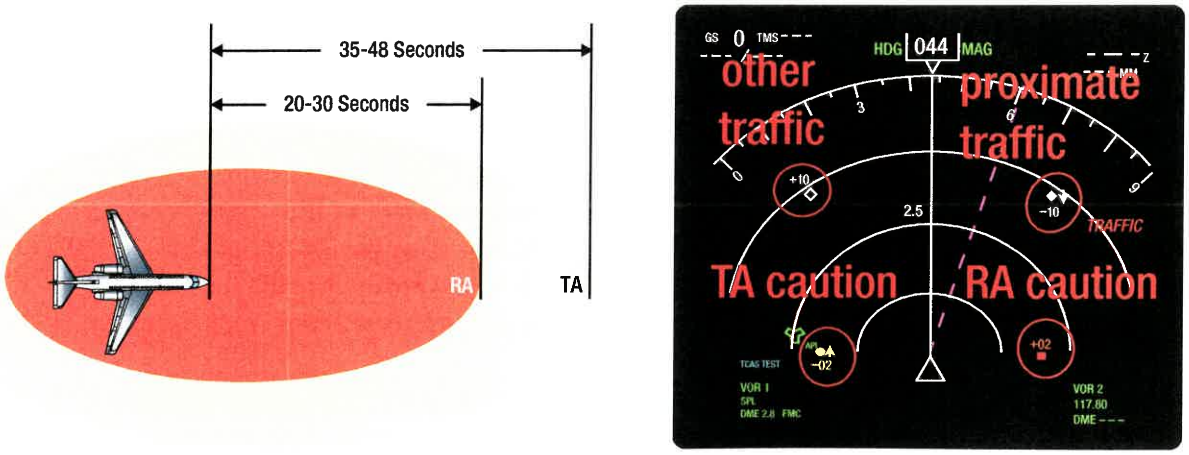


Figure 15-12. TCAS envelope (left) and TCAS display format (right).

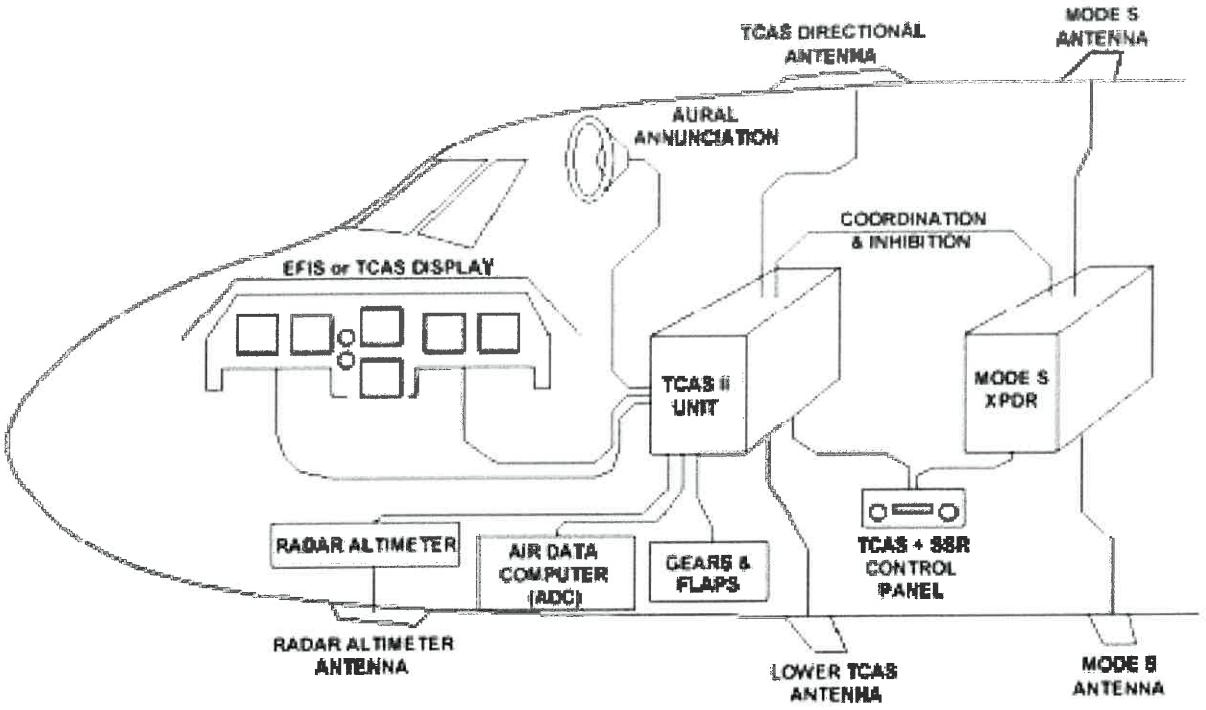


Figure 15-13. TCAS block diagram.

position and altitude of each aircraft. It does this via a directional antenna mounted on the top of the aircraft that transmits interrogations on 1030 MHz at varying power levels in each of four 90 degree azimuth segments. Transponder replies are received on 1090 MHz and sent to the TCAS computer and compared with the range and altitude data obtained from the lower antenna. The TCAS unit typically receives inputs from the air data computer and radar altimeter as well.

TCAS II equipped aircraft use continuous reply information to analyze the speed and trajectory of target aircraft in close proximity. If a collision is calculated to be imminent, an RA is issued. TCAS target aircraft are displayed on a screen on the flight deck. Different colors and shapes are used on the display to depict approaching aircraft depending on the imminent threat level. Since RAs are currently limited to vertical evasive maneuvers, some stand-alone TCAS displays are electronic vertical speed indicators.

Most aircraft use some version of an electronic HSI on a navigational page to display TCAS information. The EFIS Navigational Display or MFD may be used to depict TCAS and weather radar information simultaneously on the same screen, with the Primary Flight Display providing vertical speed commands to either ascend or descend.

AUTOMATIC DEPENDENT SURVEILLANCE-BROADCAST (ADS-B)

Collision avoidance is a significant part of the FAA's Next-Generation (Next-Gen) plan for transforming the National Airspace System (NAS). Increasing the number of aircraft using the same quantity of airspace and ground facilities requires the implementation of new technologies to maintain a high level of performance and safety. The successful proliferation of the Global Navigation Satellite System (GNSS), such as GPS, has led to the development of a collision avoidance system known as Automatic Dependent Surveillance-Broadcast (ADS-B).

ADS-B is an integral part of the FAAs Next-Gen program. The implementation of its ground and airborne infrastructure is currently underway. ADS-B is active in parts of the United States and around the world. ADS-B is available in two segments: ADS-B OUT and ADS-B IN. ADS-B OUT combines the positioning information available from a GPS receiver with onboard flight status information (i.e., location, altitude, velocity, and time). It then broadcasts this information to other ADS-B equipped aircraft and ground stations. (***Figure 15-14***)

Two different frequencies are used to carry these broadcasts with data link capability. The first is an expanded use of the standard 1 090 MHz Mode-S

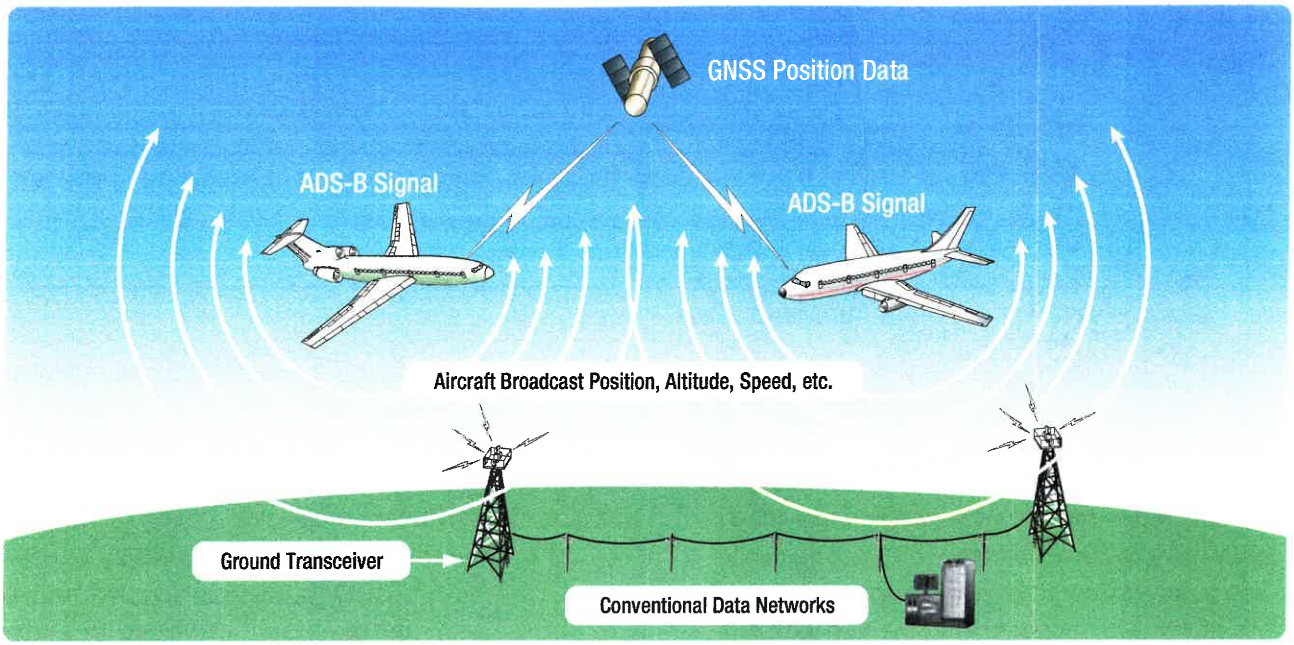


Figure 15-14. ADS-B OUT uses satellites to identify the position aircraft. This position is then broadcast to other aircraft and to ground stations along with other flight status information.

Transponder protocol known as 1 090 ES. The second, largely being introduced as a new broadband solution for general aviation aircraft is at 978 MHz using a Universal Access Transceiver (UAT). An aircraft omni-directional antenna is required in addition to the GPS antenna and receiver. Airborne receivers of an ADS-B broadcast use the information to plot the location and movement of the transmitting aircraft on an electronic display similar to TCAS. (***Figure 15-15***)

Inexpensive ground stations (compared to primary surveillance radar) are being constructed in remote and obstructed areas to proliferate ADS-B operation. (***Figure 15-16***) Ground stations share information from airborne ADS-B broadcasts with other ground stations that are part of the Air Traffic Management System (ATMS). Data is transferred with no need for human acknowledgment. Microwave and satellite transmissions are used to link the network.

For traffic separation and control, ADS-B has several advantages over conventional ground-based radar. The first is the entire airspace can be covered with a much lower expense. The aging ATC radar system that is in place is expensive to maintain and replace. Additionally, ADS-B provides more accurate information since the vector state is generated from the aircraft with the help of GPS satellites. Weather is a greatly reduced factor

Figure 15-15. A cockpit display of ADS-B generated targets (left). ADS-B airborne receiver with antenna (right).

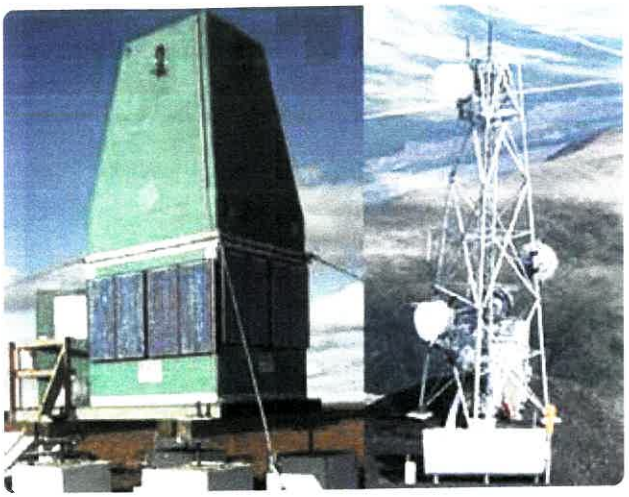


Figure 15-16. Low power requirements allow remote ADS-B stations with only solar or propane support. This is not possible with ground radar due to high power demands which inhibit remote area radar coverage for air traffic control purposes.

with ADS-B. Ultra high frequency GPS transmissions are not affected. Increased positioning accuracy allows for higher density traffic flow and landing approaches, an obvious requirement to operate more aircraft in and out of the same number of facilities. The higher degree of control available also enables routing for fewer weather delays and optimal fuel burn rates. Collision avoidance is expanded to include runway incursion from other aircraft and support vehicles on the surface of an airport.

ADS-B IN offers features not available in TCAS. Equipped aircraft are able to receive abundant data to enhance situational awareness. Traffic Information Services-Broadcast (TIS-B) supply traffic information from non-ADS-B aircraft and ADS-B aircraft on a different frequency. Ground radar monitoring of surface targets, and any traffic data in the linked network of ground stations is sent via ADS-B IN to the flight deck. This provides a more complete picture than air-to-air only collision avoidance. Flight Information Services-Broadcast (FIS-B) are also received by ADS-B IN. Weather patterns, Automatic Terminal Information Service (ATIS) information, and Notice to Airman (NOTAM) are able to be received in aircraft that have 987 MHz UAT capability. ATIS is a continuous broadcast of recorded non-ATC aeronautical information in busier terminal areas. NOTAMs are to alert pilots of potential hazards along a flight route or at a location that could affect the safety of the flight. (***Figure 15-17***)

ADS-B test units are available for trained maintenance personnel to verify proper operation of ADS-B equipment. This is critical since close tolerance of air traffic separation depends on accurate data from each aircraft and throughout all components of the ADS-B system. (***Figure 15-18***)

EMERGENCY LOCATOR TRANSMITTER (ELT)

An Emergency Locator Transmitter is an independent battery powered transmitter activated by the excessive G-forces experienced during an aircraft crash. It transmits a digital signal every 50 seconds on a frequency of 406.025 MHz at 5 watts for at least 24 hours. The signal is received anywhere in the world by satellites in the COSPAS-SARSAT (a Russian acronym translated to Space System for the Search of Vessels in Distress - Search And Rescue Satellite-Aided Tracking) satellite system. Two types of satellites, Low-Earth Orbiting (LEOSATs) and Geostationary Satellites (GEOSATs) are used with different, complimentary capability. The signal is partially processed and stored in the satellites and then relayed to ground stations known as Local User Terminals (LUTs). Further deciphering of a signal takes place at the LUTs, and appropriate search and rescue operations are notified through Mission Control Centers (MCCs) set up for this purpose.

Maritime vessel Emergency Position-Indicating Radio Beacons (EPIRBs) and Personal Locator Beacons (PLBs) use the exact same system. EPIRB beacons with built-in GPS are called GPIRBs, for GPS Position-Indicating Radio Beacon. The U.S. portion of the COSPAS-SARSAT system is maintained and operated by the National Oceanic and Atmospheric Administration (NOAA). ***Figure 15-19*** illustrates the basic components in the COSPAS-SARSAT system.

ELTs are required to be installed in most aircraft according to FAR 91.207. This encompasses most general aviation aircraft not operating under Parts 135 or 121. ELTs must be inspected within 12 months of previous inspection for proper installation, battery corrosion, operation of the controls and crash sensor, and the presence of a sufficient signal at the antenna. Built-in test equipment facilitates testing without transmission of an emergency signal. The remainder of the inspection is visual. Technicians are cautioned not to activate the ELT and transmit an emergency distress

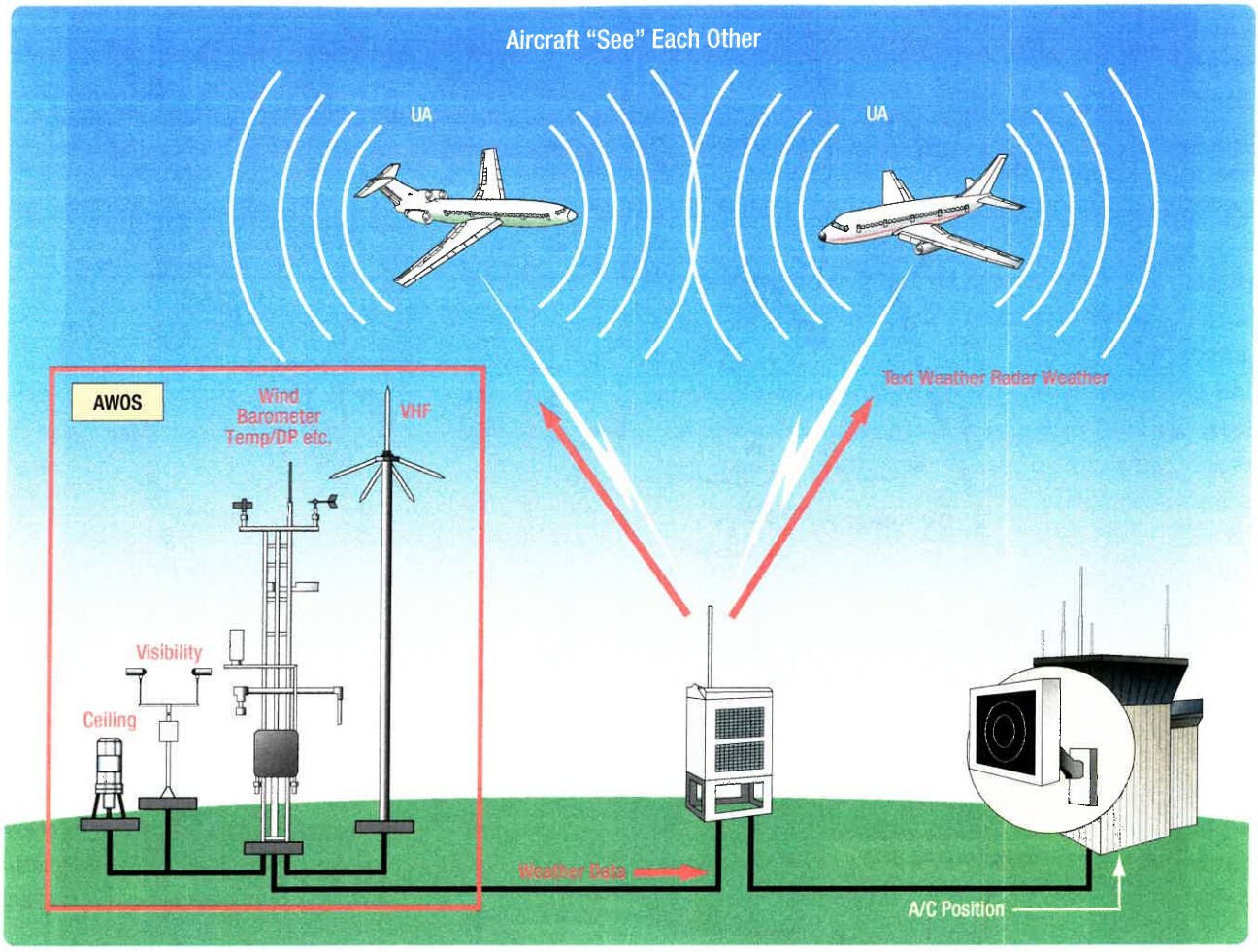


Figure 15-17. ADS-B IN enables weather and traffic information to be sent into the flight deck.

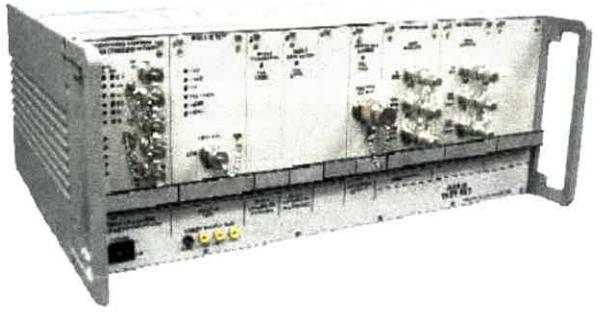


Figure 5-18. An ADS-B test unit.

signal. Inspection must be recorded in maintenance records including the new expiration date of the battery. This must also be recorded on the outside of the ELT.

ELTs are typically installed as far aft in the fuselage of an aircraft as is practicable just forward of the empennage. The built-in G-force sensor is aligned with the longitudinal axis of the aircraft. Helicopter ELTs may be located elsewhere on the airframe as they are equipped with multi-directional activation devices. Follow ELT and airframe manufacturer's instructions for proper installation, inspection, and maintenance of all ELTs. ***Figure 15-20*** illustrates ELT mounted locations.

Use of Doppler technology enables the origin of the 406 MHz ELT signal to be calculated within 2 to 5 kilometers. Second generation 406 MHz ELT digital signals are loaded with GPS location coordinates from a receiver inside the ELT unit or integrated from an outside unit. This reduces the location accuracy of the crash site to within 100 meters. The digital signal is also loaded with unique registration information. It identifies the aircraft, the owner, and contact information, etc. When a signal is received, this is used to immediately research the validity of the alert to ensure it is a true emergency transmission so that rescue resources are not deployed needlessly.

ELTs with automatic G-force activation mounted in aircraft are easily removable. They often contain a portable antenna so that crash victims may leave the site

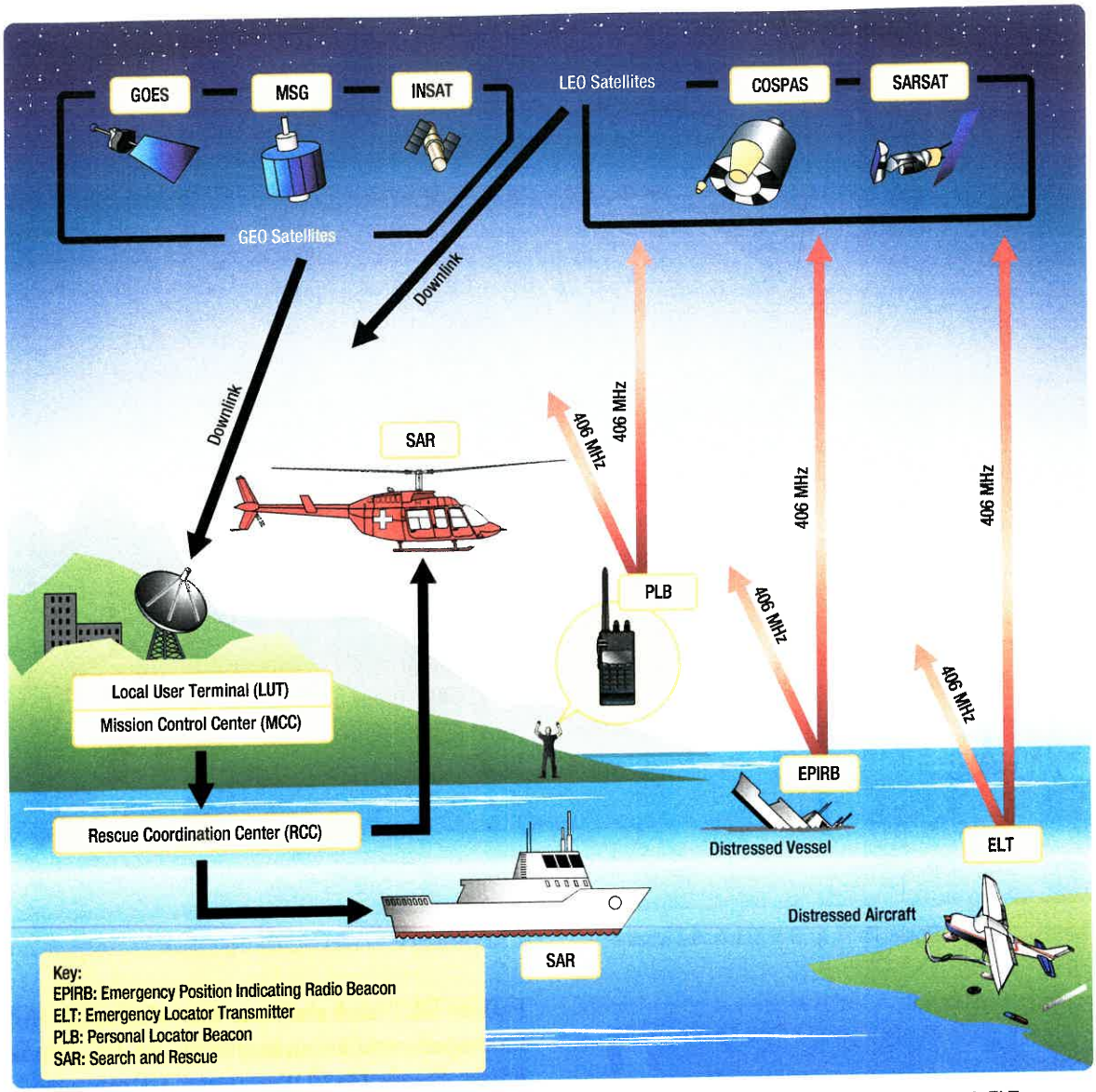


Figure 15-19. The basic operating components of the satellite-based COSPAS-SARSAT rescue system of which aircraft ELTs are a part.

and carry the operating ELT with them. A flight deck mounted panel is required to alert the pilot if the ELT is activated. It also allows the ELT to be armed, tested, and manually activated if needed. (***Figure 15-21***)

Modern ELTs may also transmit a signal on 121.5 MHz. This is an analog signal transmission that can be used for homing. Prior to 2009, 121.5 MHz was a worldwide emergency frequency monitored by the CORPAS-SARSAT satellites. However, it has been replaced by the 406 MHz standard which has not been mandated by the FAA since older 121.5 MHz ELTs satisfy the requirements of FAR Part 91.207 in all except new aircraft. Thousands of aircraft registered in the United States remain equipped with ELTs that transmit a 0.75 watt analog 121.5 MHz emergency signal when activated. The 121.5 MHz frequency is still an active emergency frequency and is monitored by over-flying aircraft and control towers instead of being received and relayed via satellite.

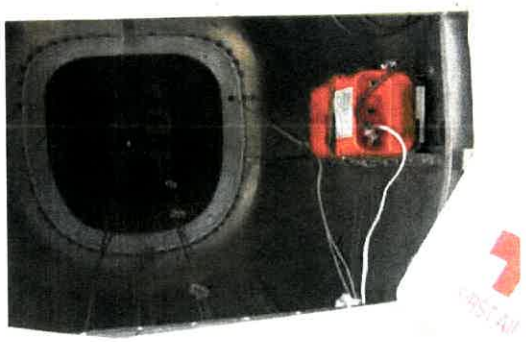


Figure 15-20. An ELT mounting location is generally far aft in a fixed-wing aircraft fuselage in line with the longitudinal axis.

Figure 15-21. An ELT and its components including a cockpit mounted panel, the ELT, a permanent mount antenna, and a portable antenna.

Technicians are required to perform an inspection and test of 121.5 MHz ELTs within 12 months of the previous one and inspect for the same integrity as required for the 406 MHz ELTs mentioned above. However, older ELTs often lack the built-in-test circuitry of modern ELTs certified to TSO C-126. Therefore, a true operational test may include activating the signal. This can be done by removing the antenna and installing a dummy load. Any activation of an ELT signal is required to only be done between the top of each hour and 5 minutes after the hour. The duration of activation must be no longer than three audible sweeps. Contact of the local control tower or flight service station before testing is recommended.

It must be noted that older 121.5 MHz analog signal ELTs often also transmit an emergency signal on a frequency of 243.0 MHz. This has long been the military emergency frequency. Its use is being phased out in favor of digital ELT signals and satellite monitoring. Improvements in coverage, location accuracy, identification of false alerts, and shortened response times are so significant with 406 MHz ELTs, they are currently the industry standard worldwide.

FLIGHT CONTROL SYSTEMS

MECHANICAL FLIGHT CONTROL SYSTEMS

Since the beginning of flight, the only means used to control the attitude, altitude, and direction of the aircraft was through push-pull control rods or cable and pulley systems from the cockpit control column and rudder pedals to the aircraft's control surfaces. (***Figure 15-22***)

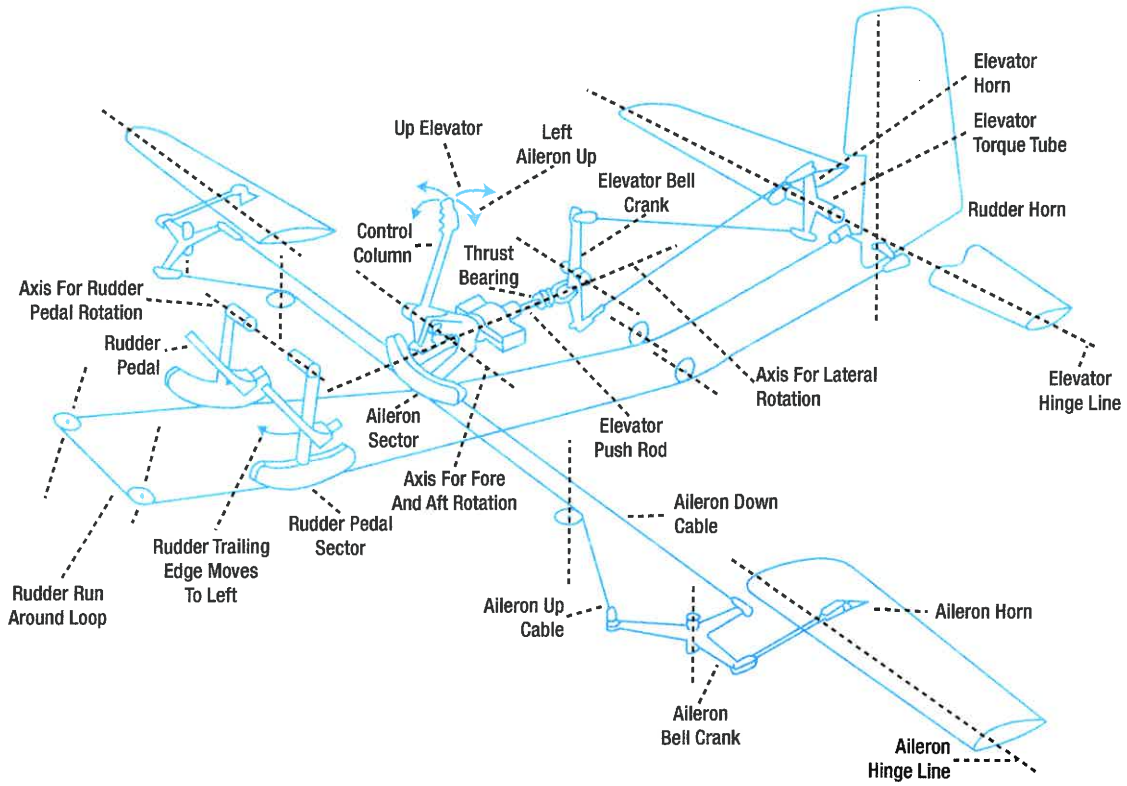


Figure 15-22. Typical mechanical flight control system.

Pitch control is exercised by the elevators located on the horizontal stabilizer to change the pitch of the aircraft. Pitch is exercised by moving the control column forward to pitch down (dive) and pulling aft to pitch up (climb). Roll control is provided by ailerons on the outboard section of the trailing edge of the wings and move in opposite directions. Roll is achieved by moving the control column to the right to drop the right wing and to the left to drop the left wing. Yaw control is provided by the rudder on the vertical stabilizer.

Pushing the left peddle will yaw the aircraft to the left, while pushing the right pedal will yaw the aircraft to the right. The roll and yaw control are used simultaneously to perform a coordinated turn to change the heading without slipping the tail. The elevator, ailerons, and rudder are known as primary flight controls.

Larger aircraft will have secondary flight controls, in addition to primary flight controls. This includes high-lift flaps located on the inboard trailing edge of the wings. Deployment of the flaps during take-off or landing extends the flap sections rearward and downward to increase wing area and camber, thereby greatly increasing lift. Slat control is provided by spoilers which extend forward and outward from the leading edge of the wings which has the effect of decreasing wing area and camber to retard lift.

At low speeds, roll control provided by the ailerons is augmented by the differential use of the spoilers. For example, during a right turn, the spoilers on the right wing will be extended to reduce the lift on that wing causing it to drop. Speed brakes are deployed when all the over-wing spoilers are extended which has the effect of further decreasing lift and increasing drag to slow the airplane upon landing prior to deploying the thrust reversers once on the ground.

The complexity and weight of mechanical Flight Control Systems (FCS) increases considerably with the size of the aircraft. Therefore, just like power-steering is used on an automobile to augment the muscular strength of the driver, hydraulic actuators were first introduced on aircraft to assist the pilot in moving the control surfaces, especially the heavy high-lift control surfaces, such as the flaps and slats. A hydro-mechanical FCS consists of a reservoir, a hydraulic pump, and network of hydraulic lines to send fluid pressure to linear actuators that move the control surface when the actuator's servo valve is opened through mechanical cables.

AUTOMATIC DIGITAL FLIGHT CONTROL SYSTEMS (ADFCS)

Hydro-mechanical systems later evolved in to Automatic Digital Flight Control Systems (ADFCS), in what has become known as "Fly-by-Wire" (FBW) flight control systems, whereby the actuator servo valves are opened by electrical signals sent from digital flight control computers. (***Figure 15-23***)

A full Fly-By-Wire system replaces the hydro-mechanical flight control system in its entirety with an electrical interface. The movements of the pilot's controls are converted to electrical signals and transmitted by wires (hence the term fly-by-wire) to the flight control computers which determine how much to move the actuators at each control surface to provide the expected response. Commands from the flight control computers are input to the actuators without the pilot's intervention in order to stabilize the aircraft during flight.

The ADFCS is a closed-loop control system meaning that the actual position of the control surface is fed back as an input signal to the flight control computer so that adjustments can be made to achieve and maintain the desired control settings.

As shown in ***Figure 15-24***, the Boeing 777 has a triple-redundant (triplex) full fly-by-wire flight control system. Position transducers change the flight crew commands of the control wheels, control columns, rudder pedals and the speed brake lever to analog signals that are sent to the Actuator Control Electronics (ACE), which convert the analog signals to digital format and sends them to the Primary Flight Computers (PFC) over three ARINC 629 data buses. In addition, the PFCs receive airspeed, attitude and inertial data from the Air Data/Inertial Reference Units.

The PFCs calculate the flight control commands based on the flight control law algorithms, and flight augmentation and envelope protection software. The digital command signals from the PFCs are sent to the ACEs. The ACEs change these command signals to analog format and sends them to the Power Control Unit (PCU) actuators which operate the control surfaces. The PCUs contain a hydraulic actuator, an electro-hydraulic

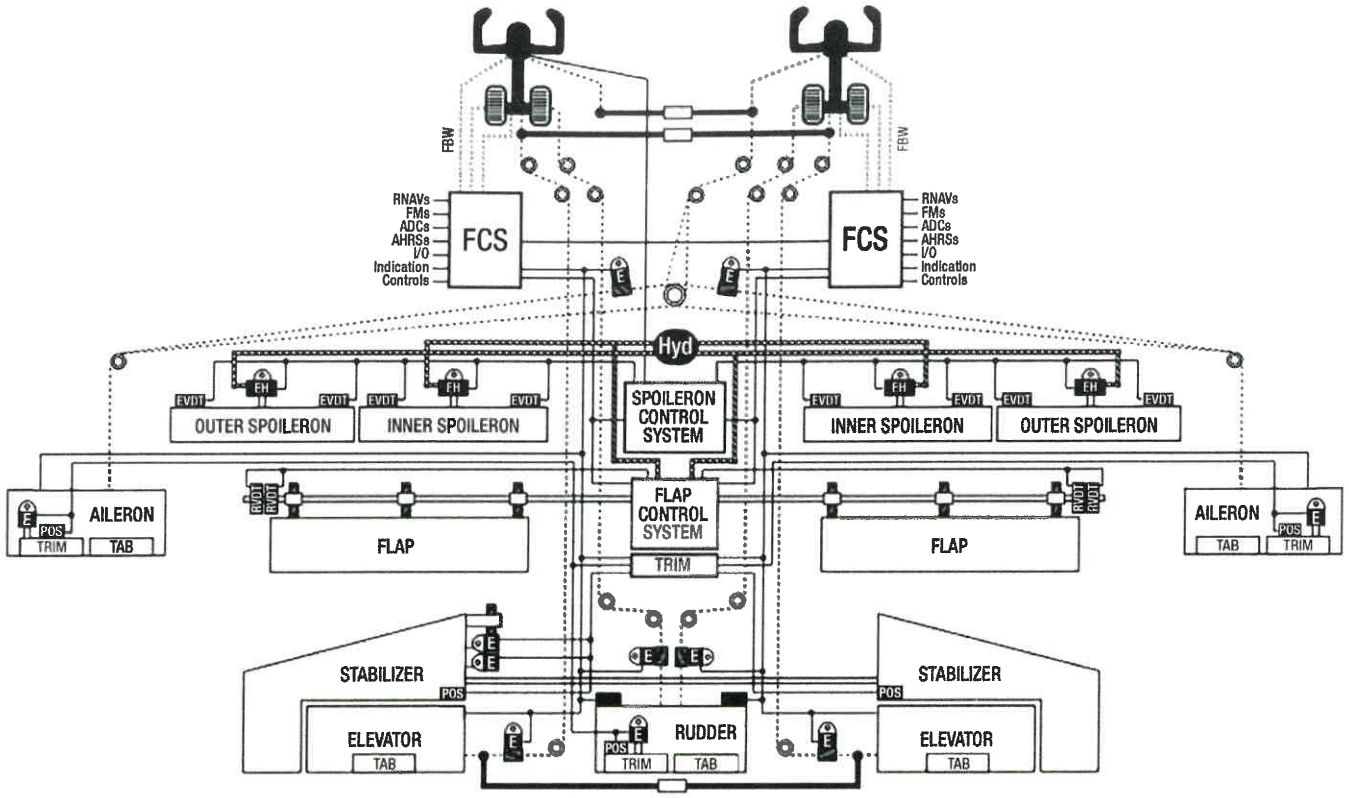


Figure 15-23. Fly-by-Wire flight control system with a mechanical backup.

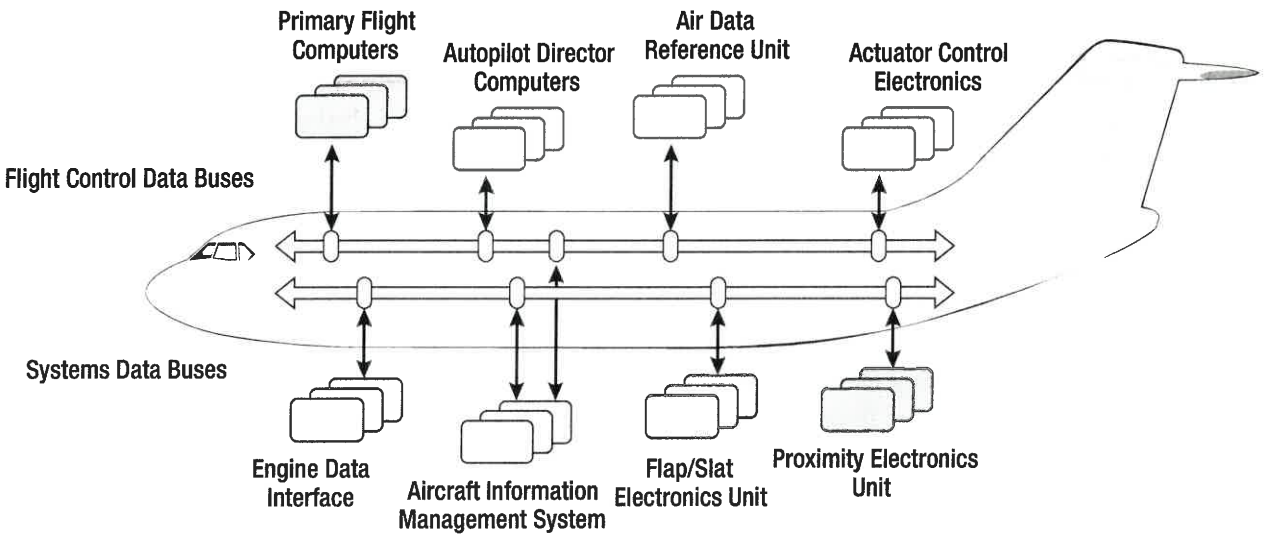


Figure 15-24. Boeing 777 Fly-by-Wire flight control system.

servo-valve, and position feedback sensors. The servo-valve causes the hydraulic actuator to move the control surface. The actuator position transducer sends a position feedback signal to the ACEs. After conversion back to digital format, the ACEs send the signal to the PFCs which stops the command when the position feedback signal equals the command position.

The PFCs receive autopilot commands from the three Autopilot Flight Director Computers (AFDCs), which receive flight navigation and guidance inputs from the FMS. The PFCs calculate the flight control commands in the same manner as done for manual operation. In addition, the PFCs supply signals to the back-drive actuators to move the control wheels, control column and rudder pedals in synchronization with the autopilot

commands to provide visual feedback of autopilot control to the flight crew. The Proximity Electronics Unit monitors the position of the landing gear, up-locks, down-locks, and all electrically controlled hydraulic selector values. It disables the brake and nose wheel well steering at takeoff and rearms them at landing.

The State-of-the-art FBW systems are using newer Electro-Hydrostatic Actuators (EHA) that have the advantage that they don't require a physical connection to the aircraft's hydraulic system to operate, thereby saving considerable weight. Each EHA (***Figure 15-25***) has self-contained hydraulic reservoirs (shown on top) and a fixed displacement hydraulic pump driven by a variable speed motor (bottom) that is controlled by the Actuator Control Electronics. EHAs are used on the Airbus A380 and Lockheed Martin F-35 Joint Strike Fighter aircraft.

CABIN SYSTEMS

A discussion on digital aircraft systems would not be complete without mentioning cabin electronics, which is familiar topic to anyone who has flown as a passenger on a modern commercial airliner. In the 1970's, In-Flight Entertainment (IFE) systems were limited to pre-recorded audio tapes or compact discs that passengers listened to through their individual earphones or headsets. Later, when flat panel LCD screens became available, passengers could watch VCR videos on their seat back color displays. (***Figure 10-16***) However, passengers today want more than pre-recorded video. They desire to use their PC laptops on board the aircraft and have an AC power source and direct internet connectivity.

Many also want cellphone connectivity while the aircraft is in flight instead of using the Air-to-Ground phone located in headrest that has limited bandwidth (3 Mbps) and restricted to use over the continental United States. For this to be possible, Wi-Fi access points and cellphone picocell base stations are being installed in aircraft that provide "hub-in-the-sky connectivity" at bandwidths over 10 Mbps via L-band or Ka-band commercial communication satellite systems (SATCOM), such as Iridium or Inmarsat.

Figure 15-25. Electrostatic Actuator used on the F-35 horizontal tail.

Figure 15-26 illustrates one such system used to provide in-flight connectivity employing a SATCOM and a low-profile electronically steerable antenna to obtain a 1500 Mhz Inmarsat broadband satellite link. The Inmarsat system has three geostationary satellites which provides adequate coverage anywhere in the world (except near the north and south poles). The satellites transmit the aircraft signals to ground stations located around the globe where the data is linked to a telecommunications provider to send the data over public networks.

On board the aircraft, a communications manager computer in the cabin acts as the server to pass the data to and from the SATCOM and distribute the data between the Wi-Fi access point, cellphone picocell, and the IFE network. Like all cellular base stations, the picocell controls the output power of the cellphone to the minimum power necessary to establish a link, thereby preventing interference with onboard aircraft systems and also preventing the cellphone from connecting to terrestrial-based cellular stations. A cockpit control is used to interrupt the system with important public address messages. The cabin crew can also send live news, sports or weather feeds. A high bandwidth data bus network, such as Firewire, is used for sending and receiving broadband video and Voice-Over-Internet Protocol (VOIP) data.

In addition to cabin applications, SATCOM transceivers are used for flight crew communications and for maintenance operations. For example, the aircraft Health and Usage Monitoring System (HUMS) constantly measures the health of all onboard systems through Built-In-Test Equipment (BITE), and if a fault is detected, it sends this information to maintenance operations via a satellite link so that the technician has a spare unit in hand to replace when the aircraft lands at its destination.

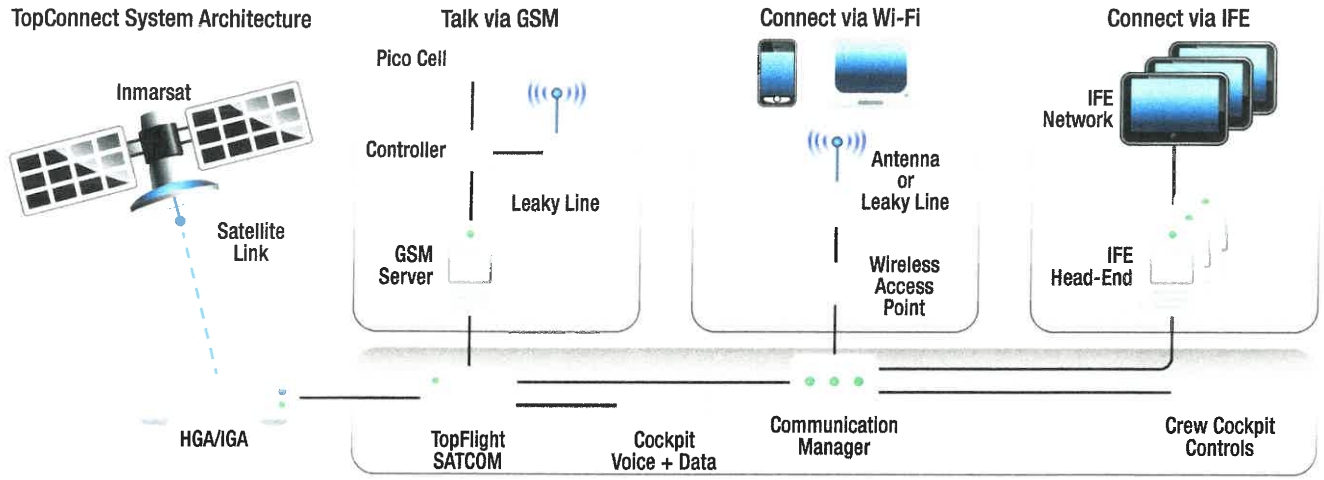


Figure 15-26. TopConnect cabin electronics system.

Question: 15-1
What are the advantages of Integrated Modular Avionics (IMA) over the traditional federated architecture approach?

Question: 15-2
What is the Aircraft Communication Addressing and Reporting System (ACARS) and why is it important for airline operations?

Question: 15-3
How does the Ring Laser Gyro (RLG) measure angular velocity or rate of turn?

Question: 15-4
How does a Global Positions System (GPS) receiver determine its location?

Question: 15-5
What is the purpose of the Wide Area Augmentation System (WAAS)?

Question: 15-6
How does the Flight Management Computer (FMC) determine the optimum flight path?

Question: 15-7
What other systems are integrated with the Flight Management Computer (FMC)?

Question: 15-8
What action should the pilot take when the Traffic Alert and Collision Avoidance System (TCAS) issues a Resolution Advisory (RA)?

ANSWERS

Answer: 15-1
The IMA concept provides a more unified approach to avionics design resulting in considerable less volume and weight due to the sharing of resources across a number of Line Replaceable Modules (LRMs). Many of the LRMs have identical hardware whose functionality differs only by the desired software application program installed. This commonality provides a pool of spare resources which improves system availability.

Answer: 15-2
Airlines pay their flight and cabin crews based on the times reported for Out of the gate, Off the ground, On the ground, and In the gate (OOOI). ACARS is a digital data link for transmission of short text messages between aircraft and ground stations to relieve the crew from having to call in their times and to provide more accurate reporting.

Answer: 15-3
Laser gyros measure angular rate by employing the properties of two laser beams inside a triangular ring-shaped tuned cavity. If the gyro was rotated on its axis, the path of one beam would be shortened, while the path for the other beam would be lengthened. The laser beam that travelled the shorter distance would increase in frequency, and the laser beam that travelled the further distance would decrease in frequency. This frequency difference, as measured by the photocell detectors at one end of the triangle, is directly proportional to angular rate of turn about the gyro's axis.

Answer: 15-4
A GPS receiver computes its distance from the satellites by measuring the travel time of the satellite's signal. By using the distances from at least three satellites, the GPS receiver can triangulate the user's current position. With measurements from four satellites, the GPS receiver can determine elevation as well.

Answer: 15-5
The WAAS provides augmentation information to GPS receivers to enhance the accuracy and reliability of position estimates. WAAS augmentation messages contain information that allows GPS receivers to remove errors in the GPS signal, allowing for a significant increase in location accuracy and reliability.

Answer: 15-6
Prior to take-off, the flight crew inputs their initial geographic location (latitude and longitude) and flight plans. The FMC receives navigation and guidance information from the air data, inertial navigation, and global positioning system, in addition to ground-based radio navigational aids, and uses that information to compute ground speed, track, wind direction and velocity. The FMC then computes the optimum flight path, using a stored digital map terrain data base, to guide the aircraft to its final destination.

Answer: 15-7
Integration with onboard radio navigational aids allows the FMC to change VOR, DME and ILS frequencies as the flight plan is enacted. Weather and traffic information is also integrated. Internal computations, using direct input from fuel flow and fuel quantity systems, allow the FMC to carry out lean operations or pursue other objectives, such as high performance operations if making up time is paramount on a particular flight.

Answer: 15-8
If a collision or near miss is imminent, the TCAS computer issues a RA. This is an aural and visual command to the pilot to take a specific evasive action. The computer is programmed such that the pilot in the encroaching aircraft receives an RA for evasive action in the opposite direction.

Question: 15-9
What is Automatic Dependent Surveillance-Broadcast (ADS-B) OUT and how is it used?

Question: 15-10
Where should Emergency Locater transmitters (ELTs) be installed in fixed-wing aircraft and how should they to be maintained?

Question: 15-11
Explain how pitch, roll and yaw control is achieved in flight.

Question: 15-12
What is a Fly-By-Wire Flight Control System?

ANSWERS

Answer: 15-9
ADS-B is an integral part of the FAA's Next-Gen program. ADS-B OUT combines the positioning information available from a GPS receiver with on-board flight status information (i.e., location, altitude, velocity, and time). It then broadcasts this information to other ADS-B equipped aircraft and ground stations.

Answer: 15-10
ELTs are typically installed as far aft in the fuselage of an aircraft as is practicable just forward of the empennage. The built-in G-force sensor is aligned with the longitudinal axis of the aircraft. ELTs must be inspected within 12 months of previous inspection for proper installation, battery corrosion, operation of the controls and crash sensor, and the presence of a sufficient signal at the antenna. Built-in test equipment facilitates testing without transmission of an emergency signal.

Answer: 15-11
Pitch control is exercised by the elevators located on the horizontal stabilizer to change the pitch of the aircraft. Pitch is exercised by moving the control column forward to pitch down (dive) and pulling aft to pitch up (climb). Roll control is provided by ailerons on the outboard section of the trailing edge of the wings and move in opposite directions. Roll is achieved by moving the control column to the right to drop the right wing and to the left to drop the left wing. Yaw control is provided by the rudder on the vertical stabilizer. Pushing the left peddle will yaw the aircraft to the left, while pushing the right pedal will yaw the aircraft to the right. The roll and yaw control are used simultaneously to perform a coordinated turn to change the heading without slipping the tail.

Answer: 15-12
A Fly-By-Wire system replaces the hydro-mechanical flight control system in its entirety with an electrical interface. The movements of the pilot's controls are converted to electrical signals and transmitted by wires to the flight control computers which determine how much to move the actuators at each control surface to provide the expected response. Commands from the flight control computers are input to the actuators without the pilot's intervention in order to stabilize the aircraft during flight.

AC	/	Alternating Current
ACARS	/	Aircraft Communication Addressing and Reporting System
ACE	/	Actuator Control Electronics (flight controls)
A/D	/	Analog-to-Digital
ADC	/	Analog-to-Digital Converter
ADF	/	Automatic Direction Finder (navigation)
ADI	/	Attitude Direction Indicator
ADS-B	/	Automatic Dependent Surveillance - Broadcast
AFCAS	/	Automatic Flight Control Augmentation System
AFDC	/	Automatic Flight Director Computer
AFDX	/	Avionics Full-Duplex Switched Network
AIMS	/	Airplane Information Management System (Boeing EIS)
ALE	/	Address Latch Enable (microprocessor)
ALU	/	Arithmetic Logic Unit (computer)
AMLCD	/	Active-Matrix Liquid Crystal Diode
APU	/	Auxiliary Power Unit
ARINC	/	Aeronautical Radio Incorporated
ATC	/	Air Traffic Control
ATIS	/	Automatic Terminal Information Service (ADS-B)
ATMS	/	Air Traffic Management System
BC	/	Bus Controller
BCD	/	Binary Coded Decimal
BIOS	/	Basic Input/Output System (software program)
BIT	/	Binary Digit
BITE	/	Built-In-Test Equipment
BM	/	Bus Monitor
CDI	/	Course Deviation Indicator
CDU	/	Control Display Unit
COPAS	/	Space System for the Search of Vessels in Distress (translation from Russian)
CPM	/	Core Processing Module
CNS	/	Communication, Navigation, and Surveillance
CMOS	/	Complementary Metal Oxide Semiconductor
CPU	/	Central Processing Unit
CRT	/	Cathode Ray Tube
D/A	/	Digital-to-Analog
DAC	/	Digital-to-Analog Converter
DC	/	Direct Current
DEMUX	/	Demultiplexer
DIP	/	Dual In-line Package (integrated circuit)
DMA	/	Direct Memory Access
DMC	/	Display Management Computer (Airbus EIS)
DME	/	Distance Measuring Equipment (navigation)
DTS	/	Data Transfer System
DRAM	/	Dynamic Random Access Memory
DU	/	Display Units
EADI	/	Electronic Attitude Direction Indicator

EASA	/	European Aviation Safety Agency
ECAM	/	Electronic Centralized Aircraft Monitor (Airbus EIS)
EFIS	/	Electronic Flight Instrument System
EHA	/	Electro-Hydrostatic Actuator (flight controls)
EHSI	/	Electronic Horizontal Situation Indicator
EICAS	/	Engine Indication and Crew Alerting System
EIS	/	Electronic Instrument System
ELT	/	Emergency Locator Transmitter
EMC	/	Electro-Magnetic Compatibility
EMI	/	Electro-Magnetic Interference
EMP	/	Electro-Magnetic Pulse
EPIRB	/	Emergency Position-Indicating Radio Beacon
EPR	/	Engine Pressure Ratio
EPROM	/	Erasable Programmable Read-Only Memory
ESD	/	Electro-Static Discharge
EUROCAE	/	European Organization for Civil Aviation Equipment
E/WD	/	Engine/Warning Display (Airbus ECAM)
FAA	/	Federal Aviation Administration
FAR	/	Federal Aviation Regulations
FBW	/	Flu-By-Wire (flight control system)
FCS	/	Flight Control System
FDM	/	Frequency-Division Multiplexing
FIS-B	/	Flight Information Services-Broadcast (ADS-B)
FMC	/	Flight Management Computer
FMS	/	Flight Management System
GB	/	Giga-Byte
GEOSAT	/	Geostationary Satellites
GHz	/	Giga-Hertz
GNSS	/	Global Navigation Satellite System
GPIRB	/	GPS Position-Indicating Radio Beacon
GPS	/	Global Positioning System (navigation)
HF	/	High Frequency
HIRF	/	High-Intensity Radiated Field
HSI	/	Horizontal Direction Indicator
I/O	/	Input and Output
IC	/	Integrated Circuit (chip)
IEEE	/	Institute of Electrical and Electronic Engineers
IFE	/	In-Flight Entertainment
IFR	/	Instrument Flight Rules
ILS	/	Instrument Landing System
IMA	/	Integrated Modular Avionics
IMU	/	Inertial Measuring Unit
INS	/	Inertial Navigation System
IRS	/	Inertial Reference System
KB	/	Kilo-Byte
LCD	/	Liquid Crystal Display

LED	/	Light Emitting Diode
LEOSAT	/	Low-Earth Orbiting Satellite
LRM	/	Line Replaceable Module
LRU	/	Line Replaceable Unit
LSB	/	Least Significant Bit
LSI	/	Large-Scale Integration (chip)
LUT	/	Local User Terminals
MAT	/	Maintenance Access Terminal
MB	/	Mega-Byte
Mbps	/	Mega-bits per second
MCC	/	Mission Control Centers
MEMS	/	Micro-Electro-Mechanical System
MFD	/	Multi-Function Display
MMU	/	Memory Management Unit
MSB	/	Most Significant Bit
MSI	/	Medium-Scale Integration (chip)
MUX	/	Multiplexer
NAS	/	National Airspace System
ND	/	Navigation Display
NOAA	/	National Oceanic and Atmospheric Administration
NOTAM	/	Notice to Airmen (FAA)
OFP	/	Operational Flight Program
OOOI	/	Out-of-the-gate, Off-the-ground, On-the-ground, In-the-gate (ACARS)
OP-AMP	/	Operational Amplifier
PC	/	Personal Computer
PCB	/	Printed Circuit Board
PCU	/	Power Control Unit (flight controls)
PFC	/	Primary Flight Computer
PFD	/	Primary Flight Display
PLB	/	Personal Locator Beacons
P-N	/	Positive-Negative (transistor junction)
PROM	/	Programmable Read-Only Memory
RA	/	Resolution Advisory (TCAS)
RAM	/	Random Access memory
RF	/	Radio Frequency
RGB	/	Read, Green, Blue (displays)
RLG	/	Ring-Laser Gyro
RMI	/	Radio Magnetic Indicator
ROM	/	Read-Only Memory
RS	/	Reset-Set (flip-flop logic circuits)
RT	/	Remote Terminal
RTCA	/	Radio Technical Commission for Aeronautics
SARSAT	/	Search And Rescue Satellite-Aided Tracking
SATCOM	/	Satellite Communications
SELCAL	/	Selective Calling
SD	/	System Display (Airbus ECAM)

SD	/	Secure Digital (nonvolatile memory card
SMA	/	Sub-Miniature version "A" (connector)
SRAM	/	Static Random Access Memory
SSI	/	Small-Scale Integration (chip)
SW	/	Software
TA	/	Traffic Advisory (TCAS)
TCAS	/	Traffic Alert and Collision Avoidance System
TDR	/	Time Division Multiplexing
TFT	/	Thin-Film Transistor
TIS-B	/	Traffic Information Services-Broadcast (ADS-B)
TMS	/	Thrust Management System
TSO	/	Technical Standard Order (FAA)
TTL	/	Transistor-Transistor Logic
UAT	/	Universal Access Transceiver (ADS-B)
ULSI	/	Ultra Large-Scale Integration (chip)
VHF	/	Very High Frequency
VLSI	/	Very Large-Scale Integration (chip)
VOR	/	VHF Omni-directional Range (navigation)
VOIP	/	Voice-Over-Internet Protocol
WDM	/	Wavelength-Division Multiplexing
WXR	/	Weather Radar
XPDR	/	Transponder (surveillance)
XOR	/	EXCLUSIVE OR (gate)

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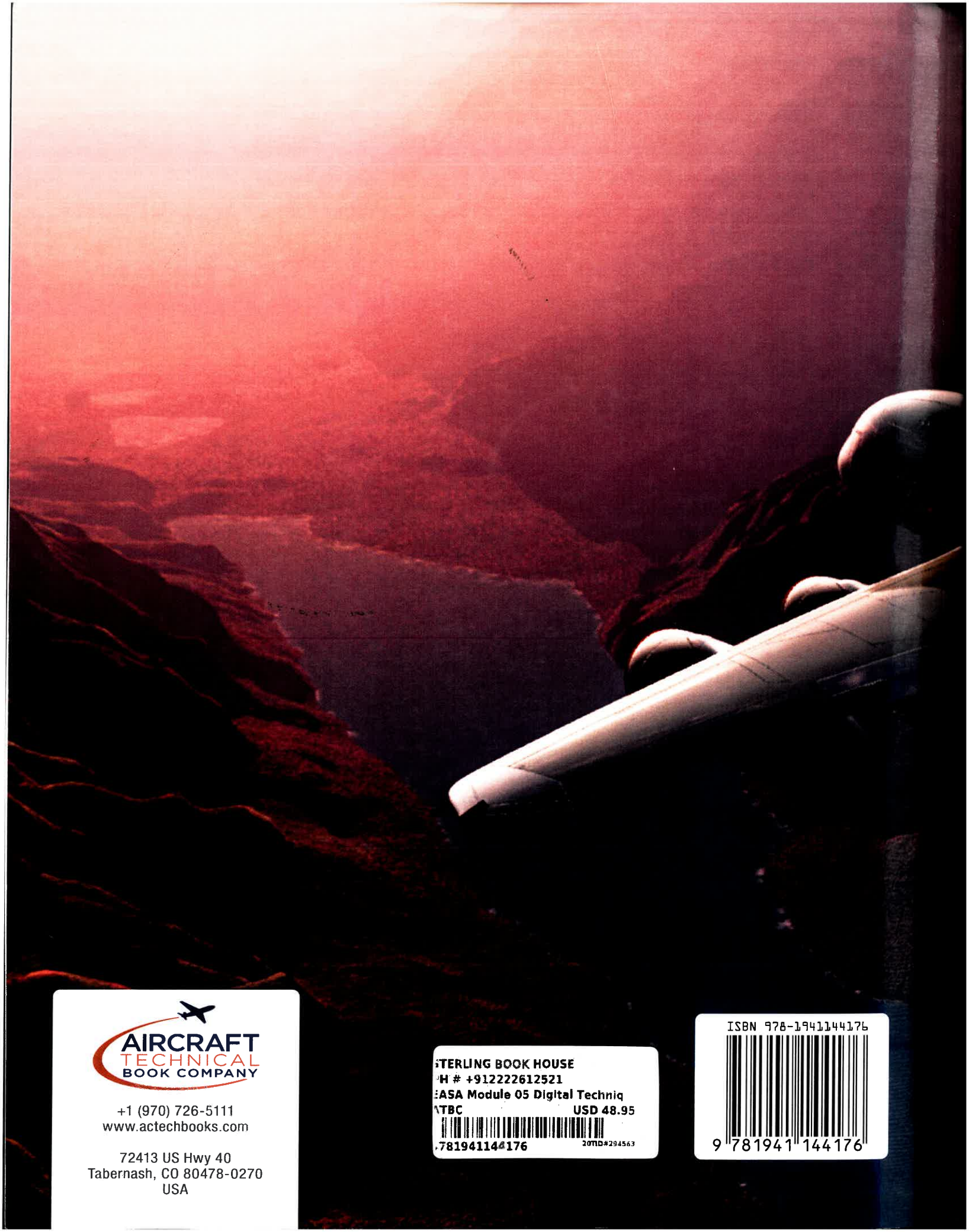

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